Differential Frequency Synchronization for PFM Using the PCIe© Common Clock

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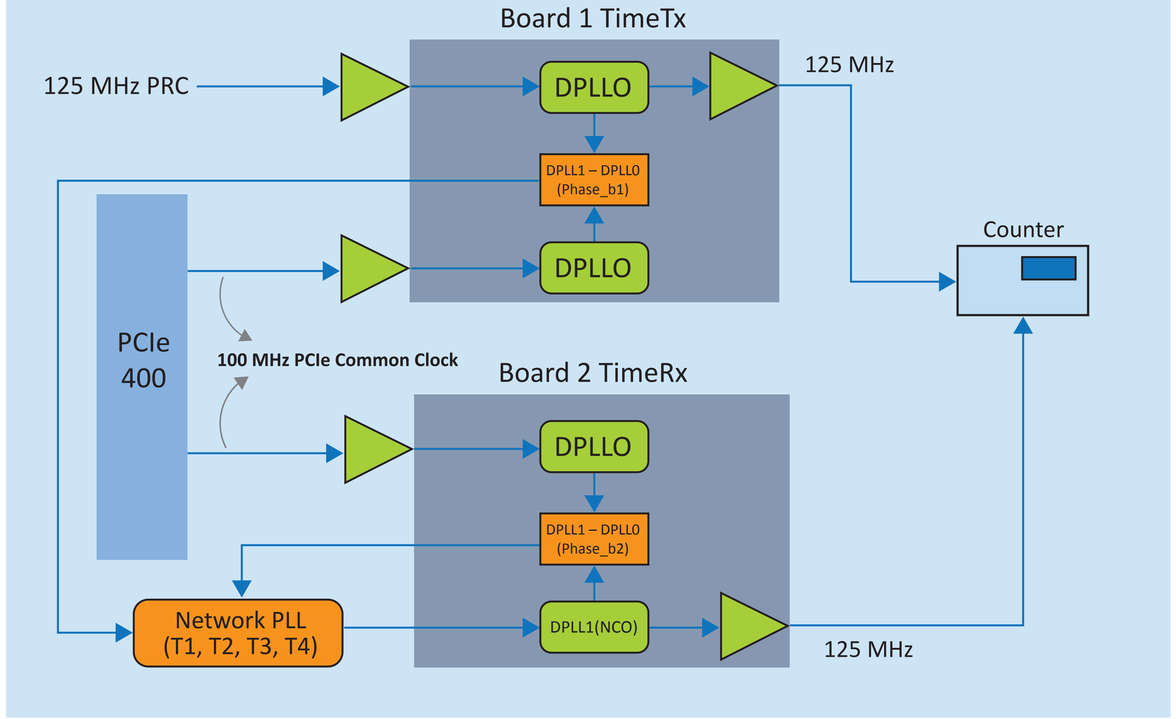
Introducing a new network Phase-Locked Loop (PLL) architecture designed for precise frequency measurement using the widely-adopted 100 MHz PCIe clock as a common reference. This approach highlights the essential role of a shared PCIe clock in achieving device synchronization across distributed networks. The new design not only simplifies interoperability but also reduces the need for additional hardware and complex synchronization protocols. By aligning measurement devices with the ubiquitous PCIe clock signal, the system ensures network-wide coherence and measurement accuracy, thereby enhancing calibration efficiency and enabling real-time frequency monitoring. This advancement significantly boosts performance and reliability in various applications that depend on PCIe technology, including high-frequency trading, telecommunications and distributed computing infrastructures.

Objectives:

- Use the 100 MHz PCIe clock as a common view reference clock.
- Increase system capacity by providing a mechanism for scaling out by adding more units.
- Use existing clock synchronization hardware and software.

Differential Clock Recovery Approach:

In the proposed setup, a TimeReceiver card and a TimeTransmitter card are synchronized using the 100 MHz PCIe common clock. To achieve precise timing alignment between the two cards, a software-based network phase-locked loop (PLL) is utilized. This PLL adjusts a numerically controlled oscillator (NCO) on the TimeReceiver card to minimize the phase difference between the two cards, ensuring that the TimeReceiver accurately tracks the frequency and phase of the primary reference clock on the TimeTransmitter card.



System Requirements:

- Multi-reference Multi-output clock generation units. These chipsets have programmable input/output frequencies using multi-DPLL configurations.
- A network synchronization software stack.

Variables:

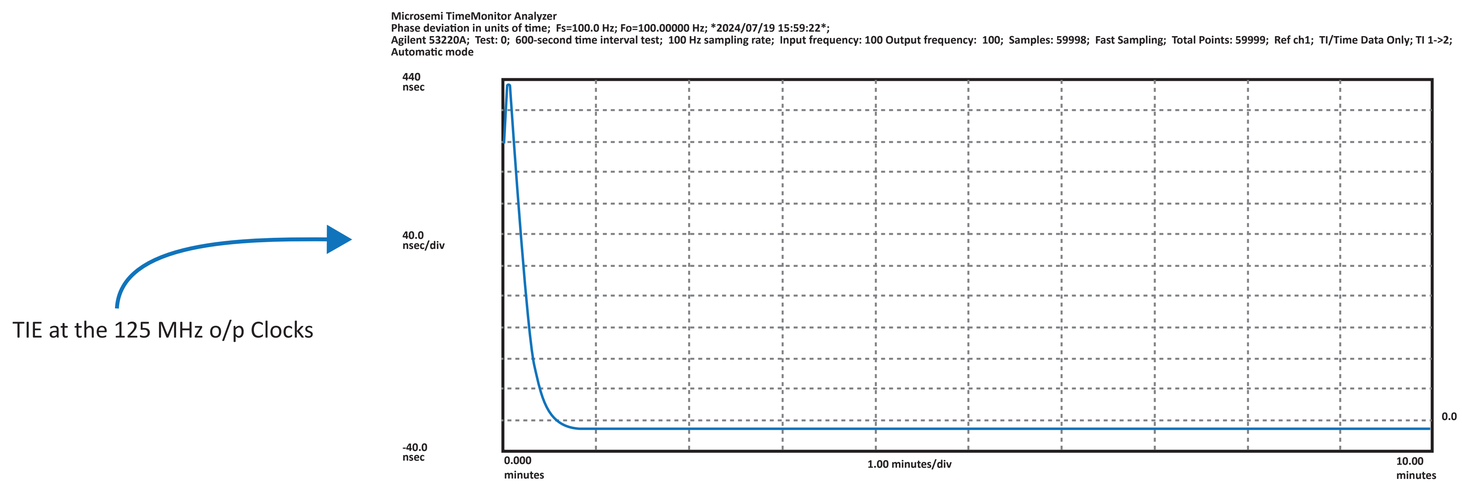
- Phase_b1: Phase diff on board 1 between reference and common clock
- Phase_b2: Phase diff on board 2 between NCO and common clock
- powerUpDiff: Initial phase offset
- transitTime: Constant communications delay between boards 1 and 2

Network PLL Timing Calculations:

- T1 = currentTime + Phase_b1 – powerUpDiff
- T2 = currentTime + phase_b2 + transitTime
- T3 = currentTime + Phase_b2
- T4 = currentTime + (Phase_b1 - powerUpDiff) + transitTime

Lab Performance:

- Frequency Offset between PCIe clockand PRC is 300 ppm
- Phase acquisition rate is 8 Hz
- OCXO on Board 1 offset is 5 ppm
- OCXO on Board 2 Offset is 100 ppb



TIE at the 125 MHz o/p Clocks