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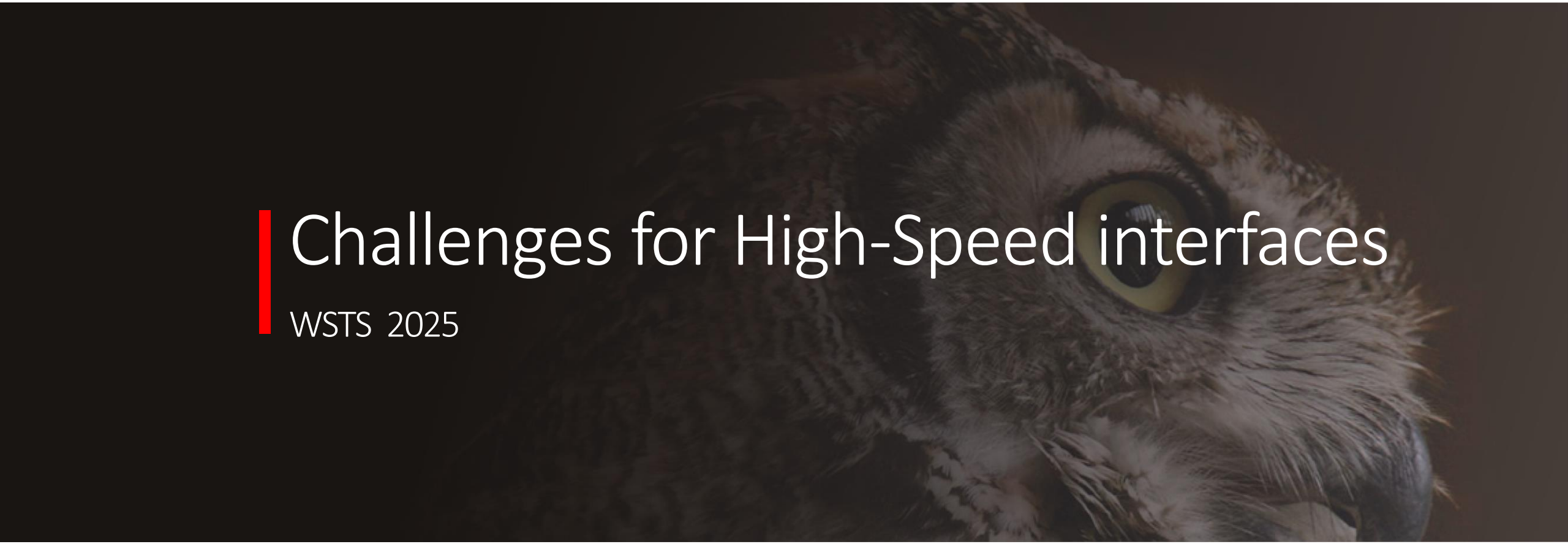

Challenges for High-Speed interfaces

WSTS 2025

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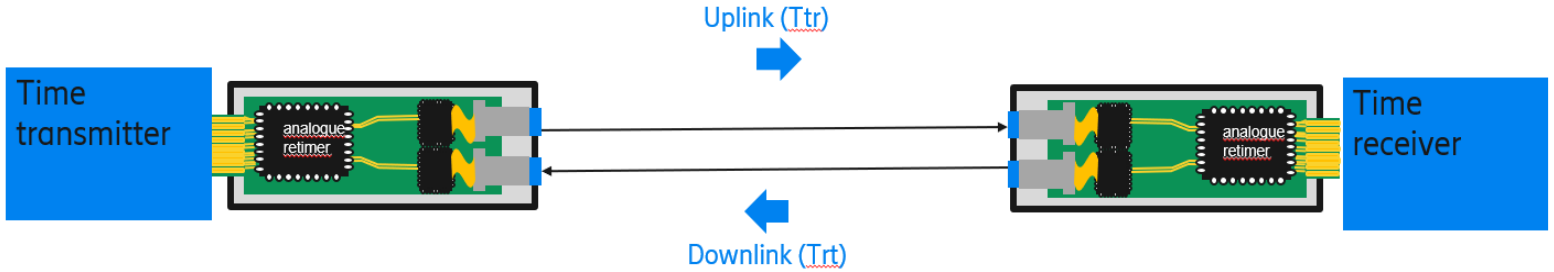
Contents

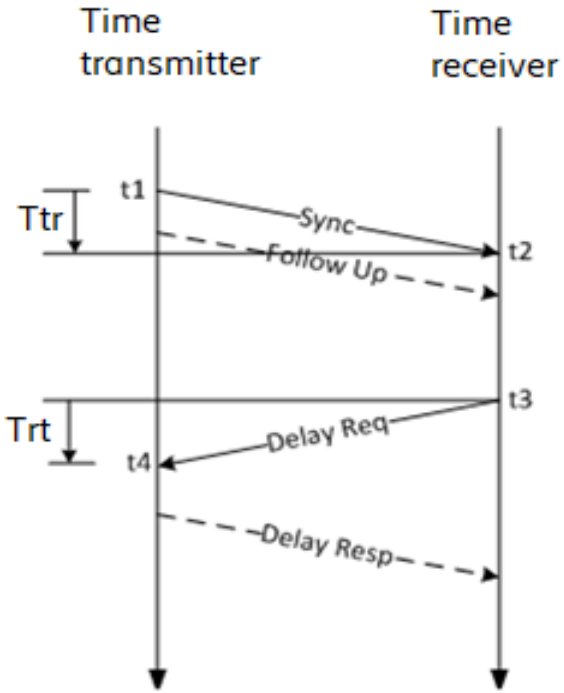
- Introduction
- Standardization Aspects
- Test results
- Conclusions

Time Sync challenges

- Delivery of synchronization across the network is key to operation and performance of many services
  - Telecoms, Power Utilities, Industrial Automation, Data Centers, Multimedia
- Increase in data rate leads to introducing new optical interfaces in transport network, that ultimately are part of the synchronization network.
- Asymmetries and change of Asymmetries at any change in the network have a direct impact on the time sync performance

Time Error (Asymmetries) in Fiber Optics





Delay = [(t2 – t1) + (t4 - t3)] / 2 = **(Ttr + Trt) / 2**

Offset = t2 - t1- Delay = **Ttr – Delay**

*If Ttr and Trt are different, half the difference becomes **time synchronization error** for the time receiver*

Sources of delay differences in Fiber optics:

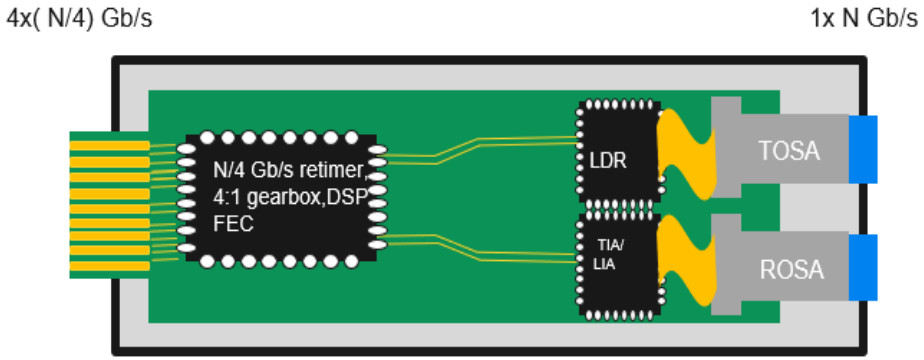
- Fiber length (every meter contributes by 5 ns; e.g., patch cords)
- Chromatic dispersion (e.g., 0.3 ns per Km, see G.652)
- System Internal optical components (e.g., WDM filters, 1-10 ns)
- Optical transceivers and Digital IC

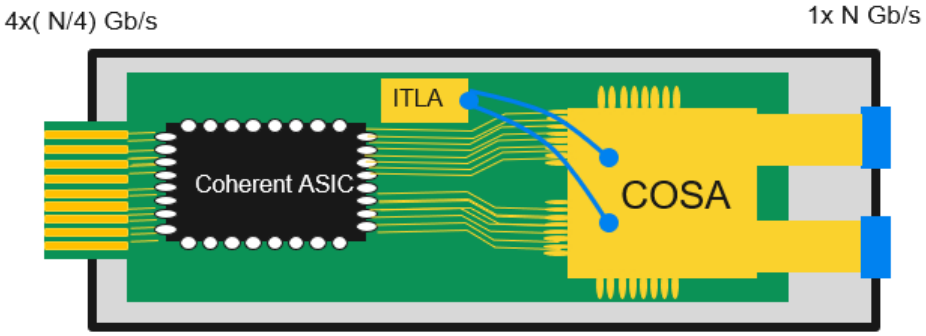
Material from :
MOPA_Tight-Sync_Paper-v1.0.pdf (mopa-alliance.org)

MOPA, Mobile Optical Pluggable Alliance is an industry effort publishing technical papers describing all relevant high-level requirements and optical solution “Blueprints” for mobile optical transport

Pluggables with increasing complexity

- Potential source of time error in complex digital parts of pluggables.
- Higher bit rates (50 Gb/s and higher) and adoption of advanced modulation formats (PAM-4, Coherent), require complex digital signal processors (DSPs) in optical pluggables.
  - A DSP converts analogue signals into digital and implements complex signal processing functions. In the Tx case, it can also convert the signal back to analogue to drive the optical transmitter.
  - The presence of DSPs can potentially make Ttr and Trt significantly different.
  - In some cases, even more complex digital functions like gear-boxing, framing and FEC (Forward Error Correction) can be implemented in the DSP and they could dominate the contribution of optical pluggables)





Transmitter Optical Sub-Assembly: TOSA
Receiver Optical Sub-Assembly : ROSA
Coherent Optical Sub-Assembly : COSA

Relationship with clock specifications

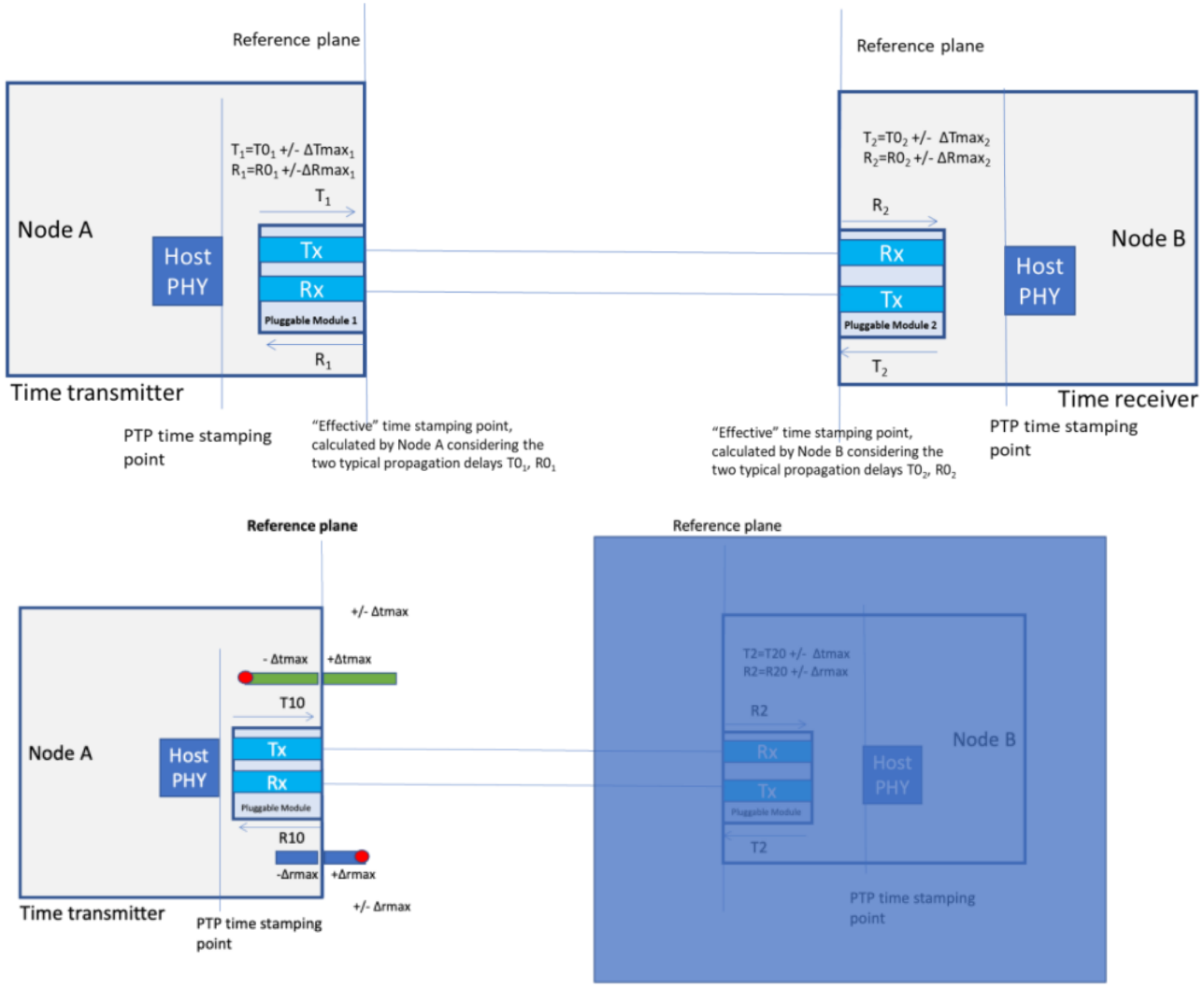


Figure APB.9: Time transmitter side average and delta propagation delay values.

Figures from
[MOPA_Tight-Sync_Paper-v1.0.pdf (mopa-alliance.org)]

ITU-T recommendations specifies requirements at Node level, as measurable on the external interfaces (contribution from -a pair of- pluggables is part of it)

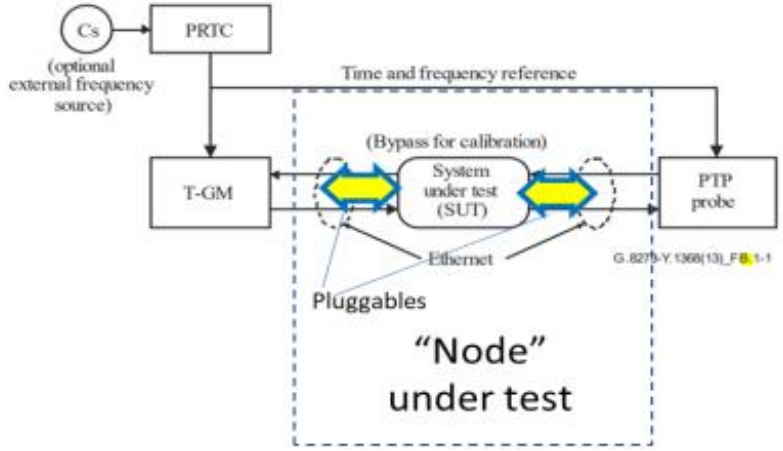
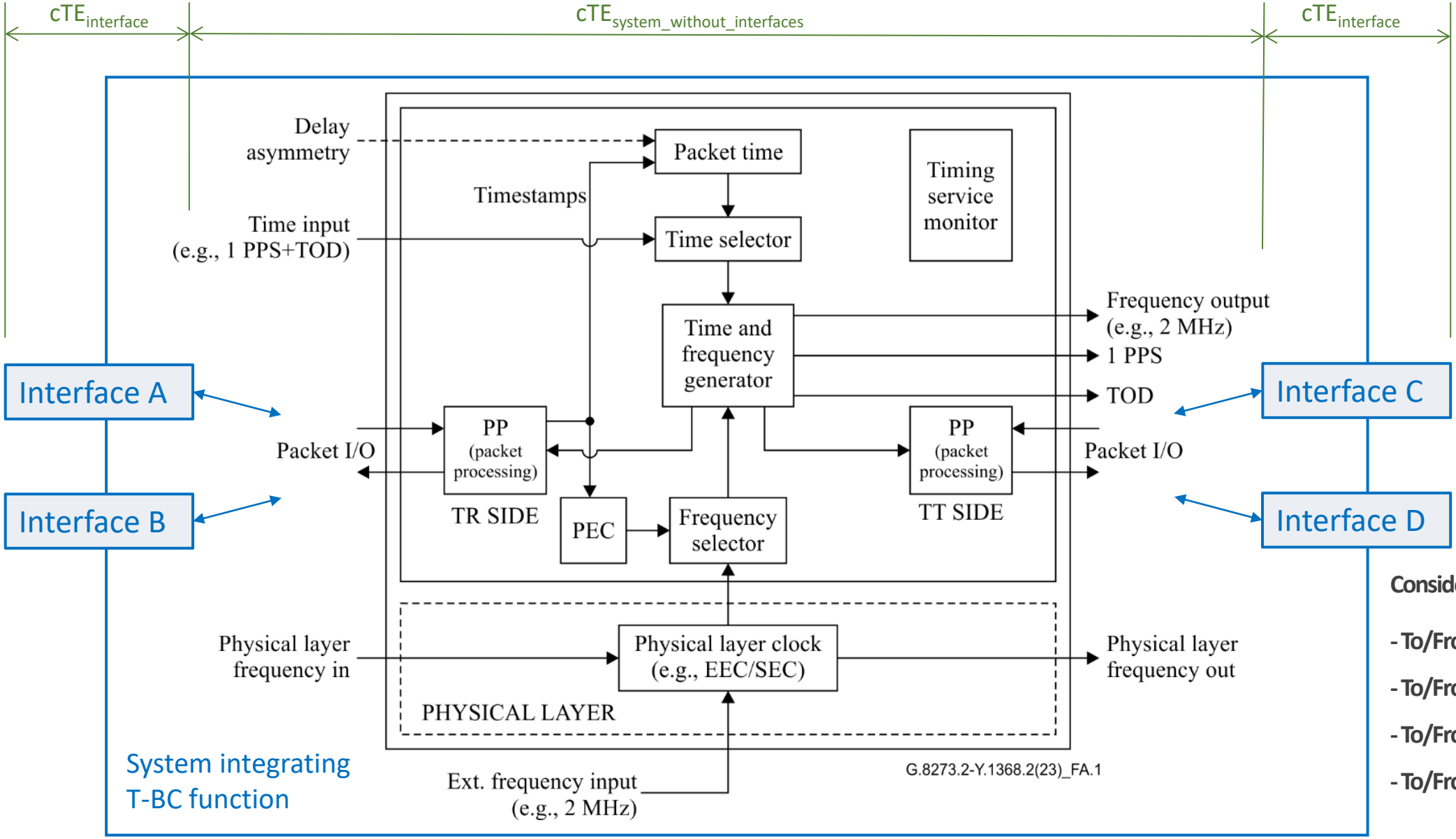


Figure APB.6 from MOPA Technical Paper
(based on Figure B.1.1 from G.8273 Annex B)

Different T-BC classes supported by an implementation

Interface A, C: high performance interface (e.g., cTE < 2 ns, negligible dTE)
Interface B: medium performance interface (e.g., cTE < 10 ns, negligible dTE)
Interface D: lower performance interface (e.g., cTE < 30 ns, negligible dTE)



Considerations on feasibility:

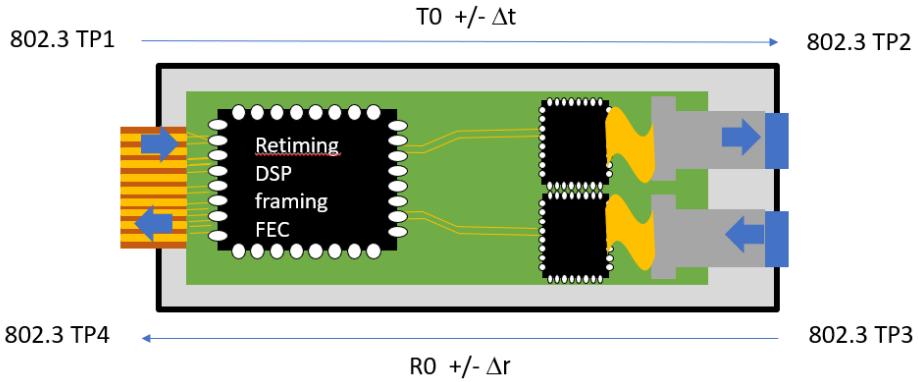
- **To/From A to C: Class C**
- **To/From A to D: Class A**
- **To/From B to C: Class B**
- **To/From B to D: Class A**

Latency Compensation, MOPA approach

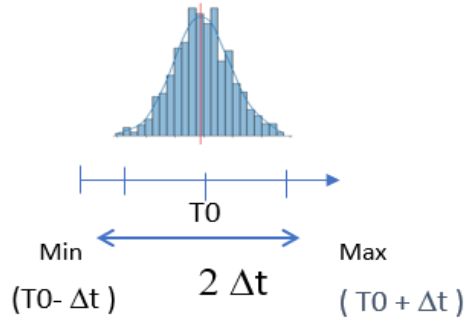
Static part “Quasi-static” part

T = T0 +/- Δtmax

R= R0 +/-Δrmax



*These values can be measured during **Design Validation Testing** (DVT), by grabbing a population of transceivers and measuring Tx and Rx propagation delays at corners and several times after link re-start conditions.*



T0 = mean propagation delay at BOL

Δt = **3σ**

T0, R0 can be stored in transceiver’s EEPROM and **compensated for at node level.**

Δtmax and Δrmax contribute to the worst case cTE, which for a **single** pluggable is

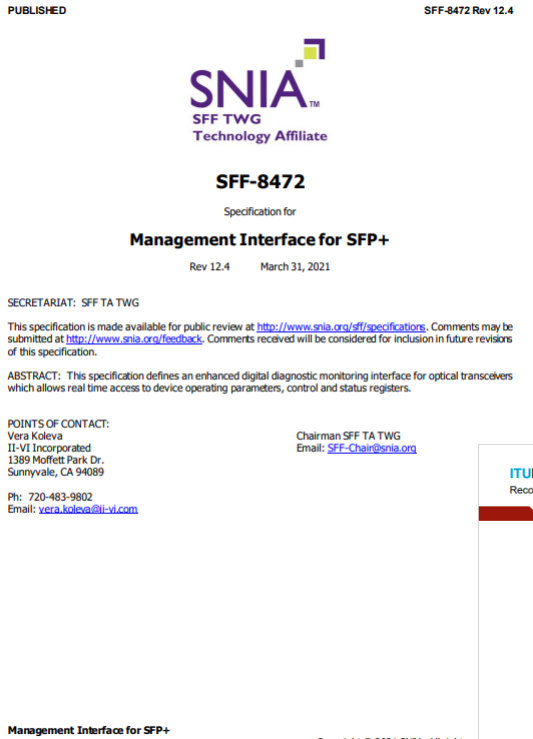
cTE max = +/- ½ (Δtmax + Δrmax)

“Constant” (“not varying in-service”) seems suitable for pluggable optics: once an optical link is operational, the propagation delay asymmetry introduced by pluggables does not change significantly

New Requirements in standards

- Classes of pluggables in ITU-T G.8273.2 and G.8273.3

- EEPROM Data Structure in relevant standards (e.g., SNIA SFF 8472)



PUBLISHED SFF-8472 Rev 12.4

SNIA
SFF TWG
Technology Affiliate

SFF-8472

Specification for

Management Interface for SFP+

Rev 12.4 March 31, 2021

SECRETARIAT: SFF TA TWG

This specification is made available for public review at http://www.snia.org/sff/specifications. Comments may be submitted at http://www.snia.org/feedback. Comments received will be considered for inclusion in future revisions of this specification.

ABSTRACT: This specification defines an enhanced digital diagnostic monitoring interface for optical transceivers which allows real time access to device operating parameters, control and status registers.

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Management Interface for SFP+

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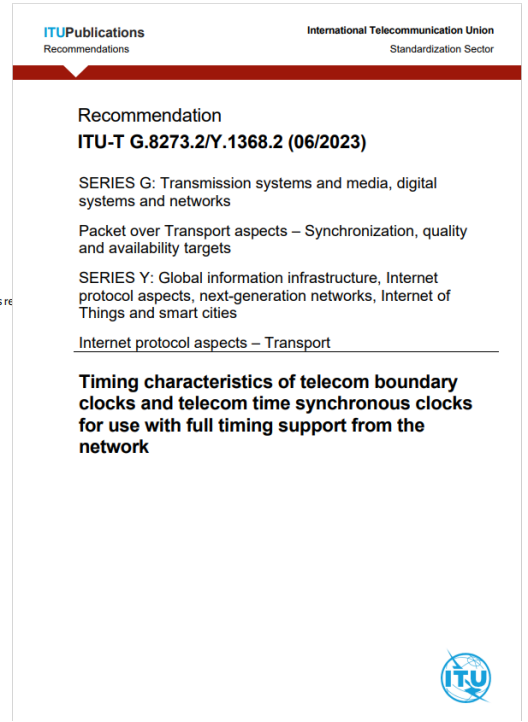


ITUPublications
Recommendations

International Telecommunication Union
Standardization Sector

Recommendation
ITU-T G.8273.2/Y.1368.2 (06/2023)

SERIES G: Transmission systems and media, digital systems and networks

Packet over Transport aspects – Synchronization, quality and availability targets

SERIES Y: Global information infrastructure, Internet protocol aspects, next-generation networks, Internet of Things and smart cities

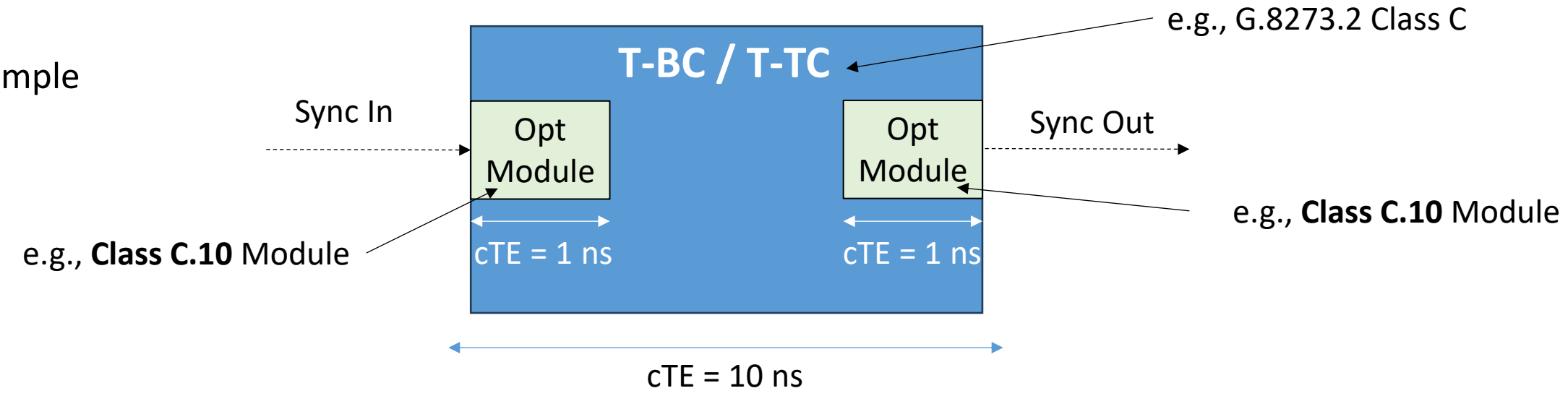
Internet protocol aspects – Transport

Timing characteristics of telecom boundary clocks and telecom time synchronous clocks for use with full timing support from the network

Standardized Performance

- Classes of pluggables in the clock specifications based on MOPA proposed approach
  - Informative Appendix (typically the normative requirements are specified for the entire system) with examples of Optical module classes suitable to meet the requirements for a specific class of clock
  - The latency class of the pluggable module (in a given mode) is deduced from the maximum of its ΔTmax and ΔRmax values

Example



8 ns can be allocated to other parts of the system (system clock, internal timing distribution, etc.)

New Appendix in G.8273.2

Appendix XII

Impact on timestamping accuracy caused by optical pluggables

(This appendix does not form an integral part of this Recommendation.)

T-BC/T-TSC performance specified in clause 7 includes time error caused by the physical interface, highlighted in table 7-1 NOTE 1. Typically, the interfaces consist of optical pluggables which are detachable devices and not necessarily delivered with the network element implementing a T-BC/TSC but is rather plugged into the network element when deployed.

The Mobile Optical Pluggable Alliance (MOPA) document [b-MOPA1] describes aspects that impact time accuracy in optical pluggables.

In order to control the impact on the time error in optical pluggables, MOPA propose in [b-MOPA2] to classify the optical pluggables based on their time error impact as a percentage of the constant time error budget of a T-BC/T-TSC (e.g., class C.10 that is read out as 10% of the cTE for a class C clock), see table APB.2 in [b-MOPA2].

To compensate for known asymmetry in an optical pluggables, it is proposed in clause 7.1 of [b-MOPA2] to store known transmit and receive delays in the optical pluggables, this information can then be then used to compensate the timestamps and hence reduce the time error.

	Class A.10	Class A.20	Class B.10	Class B.20	Class C.2	Class C.10
Max constant time error budget allocated to one pluggable	+/- 5ns	+/-10ns	+/- 2ns	+/- 4ns	+/- 0.2ns	+/- 1ns
	ΔTmax=+/-5ns	ΔTmax=+/-10ns	ΔTmax=+/-2ns	ΔTmax=+/-5ns	ΔTmax=+/-0.2ns	ΔTmax=+/-1ns
	Δmax=+/-5ns	Δrmax=+/-10ns	Δrmax=+/-2ns	Δrmax=+/-5ns	Δrmax=+/-0.2ns	Δrmax=+/-1ns

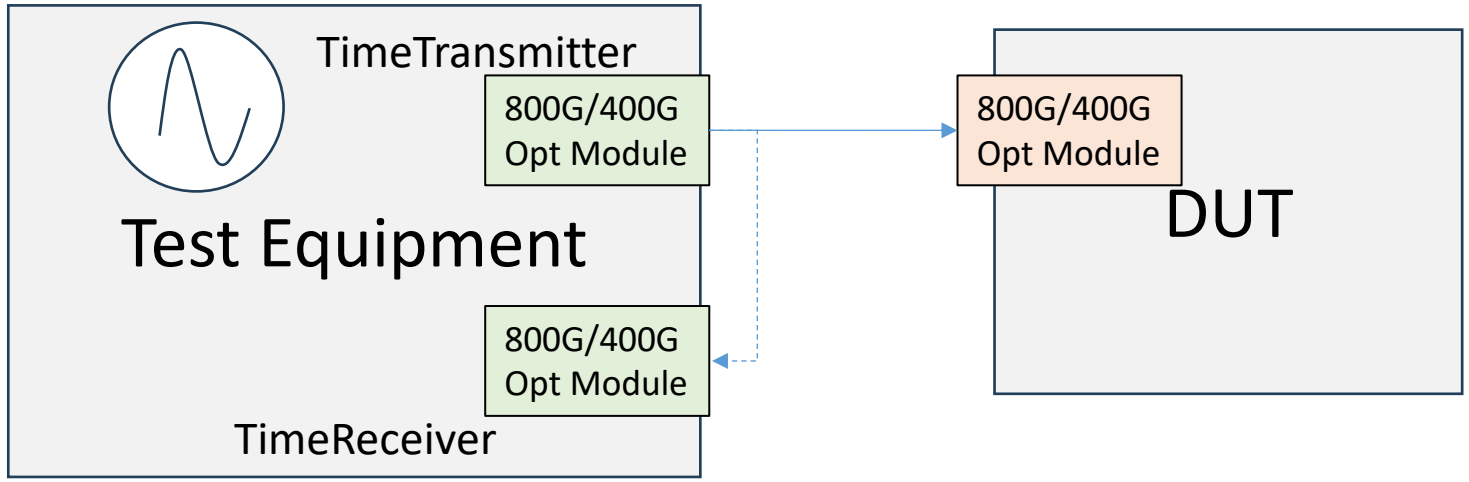
Table APB.2: Proposed optical pluggable classes.

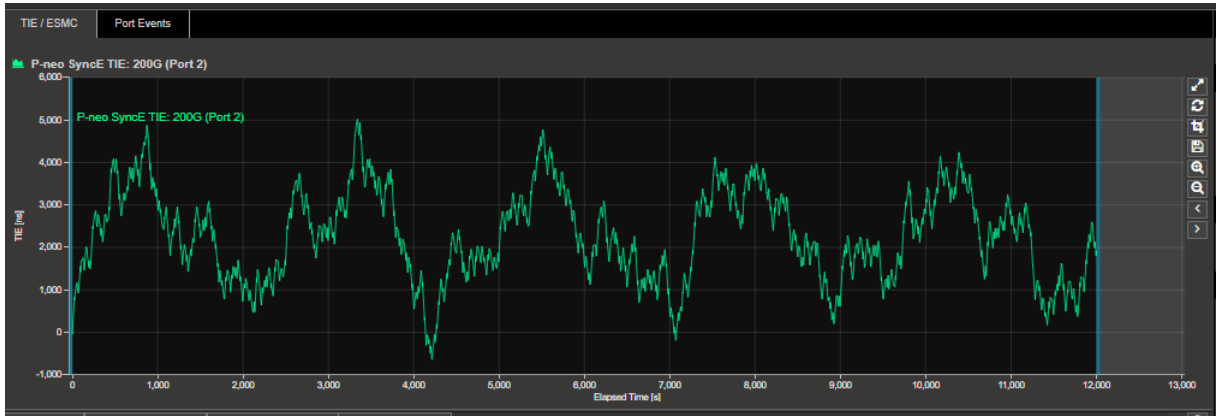
TAble from
MOPA_Tight-Sync_Paper-v1.0.pdf (mopa-alliance.org)

800G / 400G Optical module tolerance to Frequency error

- **800G** optical modules would typically drop link on the Rx side with a step in frequency from 0ppm -> **+/- ~10ppm** or more is encountered.
- Similar testing of **400G** QSFP-DD modules had a better tolerance with Rx link dropping with 0ppm -> **+/- ~38ppm** stimulus
- Tolerance without optics (i.e., electrical cable loopback) with tolerance well beyond these range, proving the weakest link was the optical modules.

Results from early samples





Sequence of input stimulous results in frequency changes at the DUT input: cosine frequency modulation introduces a step change from 0ppm to a max freq which can potentially be greater than what optical modules can tolerate

LPO (Linear Pluggable Optic)

- LPO (Linear Pluggable Optics) solution for power savings for optical interconnect by removing the digital signal processing (DSP) function from the pluggable optical module, see www.lpo-msa.org
- This also allows to reduce latency …

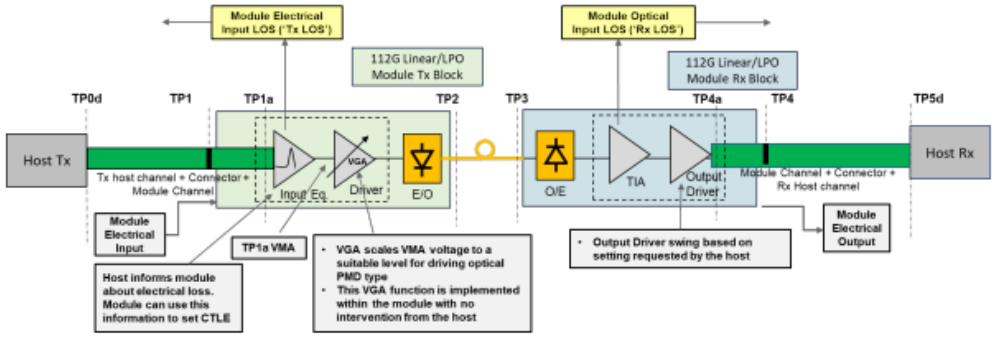
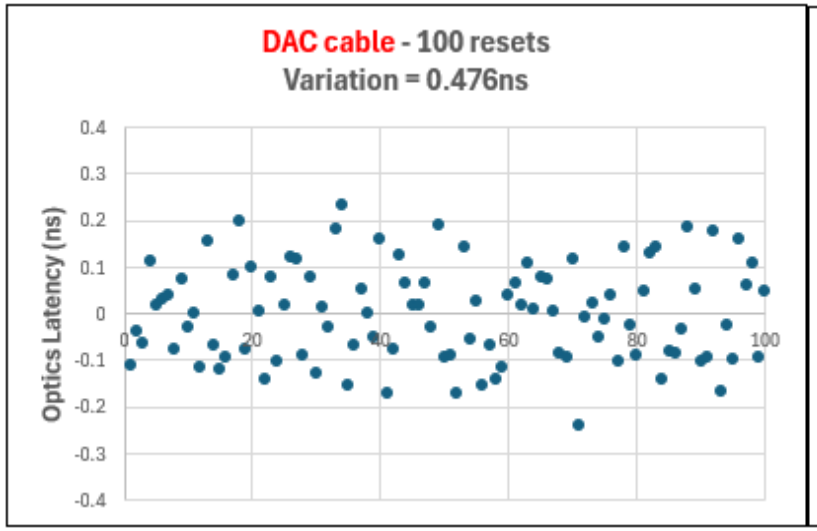
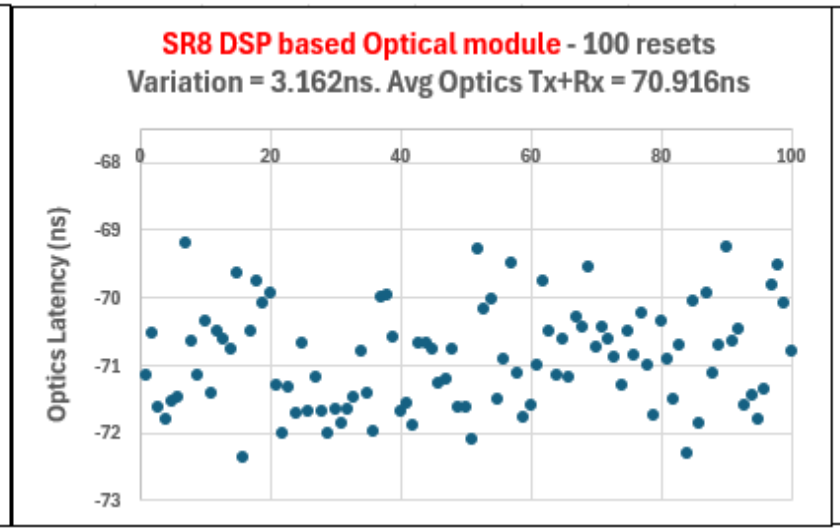
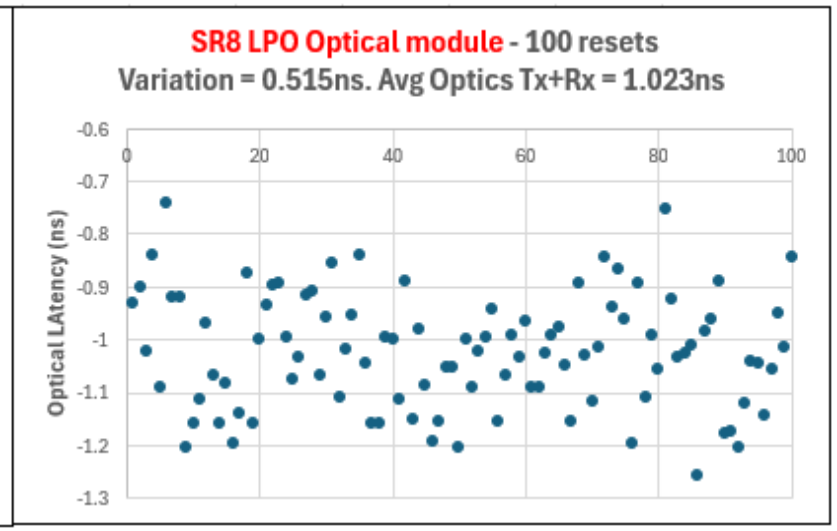


Figure 2: System Block Diagram

From LPO-MSA Specification

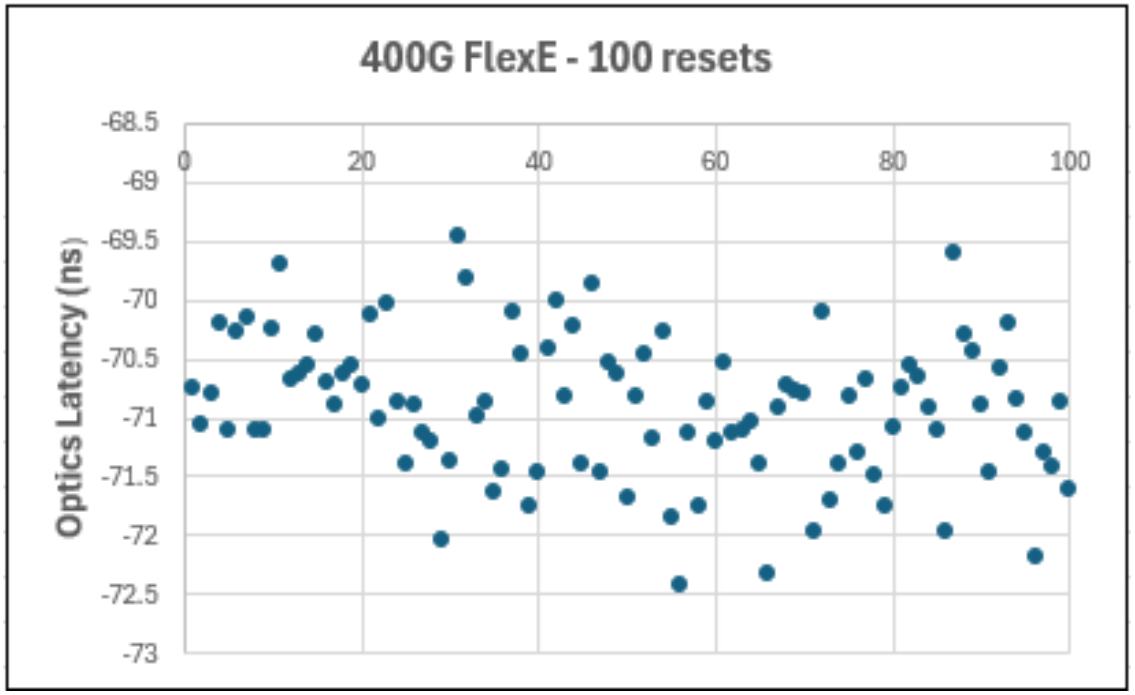


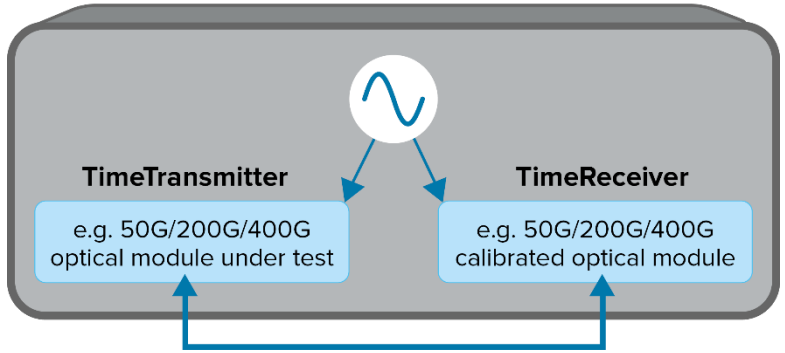




- Good results from on Time Error, but moving the complexity into the host ?
  - DSP will still be used in the optical modules for some time unless short fibers are used (BER issue).

FlexE (400G)





- Significant Total «Tx + Rx» latency
- Asymmetries expected (Measurements ongoing)

- FlexE resolve some aspects compared to Ethernet (e.g., impact from Idle insertion/removal, alignment marker/codeword marker insertion/removal, etc.), but optical impact remains ...
- Timing (PTP) impacted with similar issues (same impact from optical modules expected)

Summary

- The increase in data rate leads to introducing new optical interfaces in transport network
  - The complexity of these interfaces may result in degradation of the timing accuracy
- Interfaces that present most criticalities are due to use of DSP and use of higher bit rates: time asymmetries and reduced tolerance to frequency error
  - LPO hope for the future
  - Important to be able to characterize the performance of the interfaces
- Standardized solutions will address some of the key issues

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