High Accuracy
Revolution or Evolution?

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

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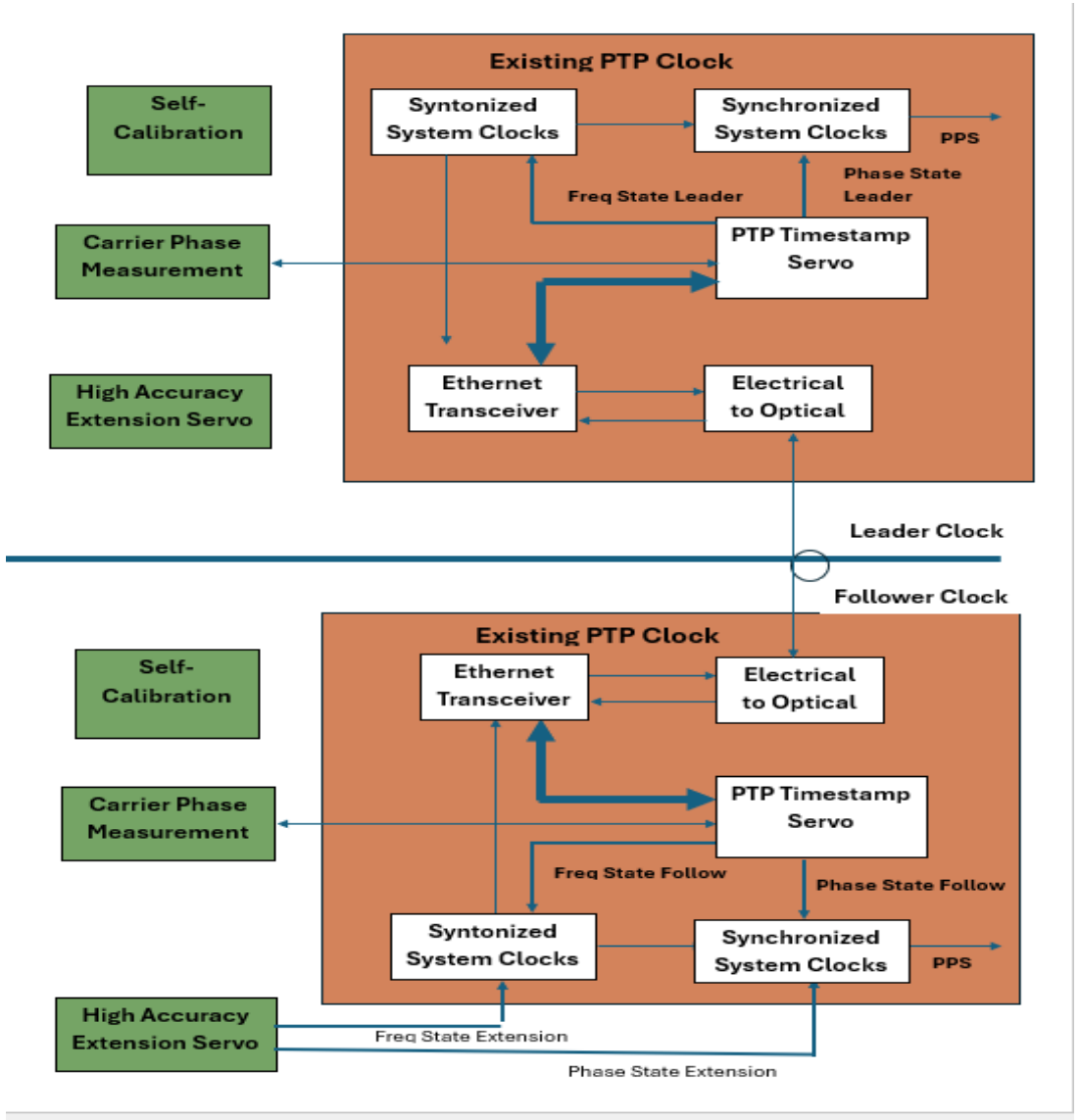
Evolutionary High Accuracy Design

- Existing PTP Clock “red block”
- Green blocks show extensions for high accuracy
- Extensions require only a software upgrade
- PTP clock hardware needs to meet sensible requirements



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High Accuracy

Several Levels Available

- **Class D (5ns Time Error) Boundary Clocks**
  - Widely deployed in virtual PRTC (vPRTC) horseshoe architectures with multi-domain high performance boundary clocks and ePRTC with east-west directions for redundancy, using Optical Timing Channel (OTC) or Optical Supervisory Channel (OSC)
- **Enhanced High Accuracy (better than class D)**
  - Requires world class synthesizer
  - Enhanced hardware platform leads to accuracy levels of 1.7ns (2.5x better than class D)
  - The one that can be supported with enhanced hardware with worldclass synthesizer (1.7ns for instance)
- **High Accuracy Time Transfer (HA-TT)**
  - Using enhanced hardware platform with world class synthesizer
  - High Accuracy extension servo
  - Meets 5ns time error over 800 km (equates to 500ps per hop assuming 10 hops of 80km each)

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Existing PTP Clock Preferred Design

- IEEE 1588 high accuracy standard recommends the use of syntonized clocks “same rate”
- An ultra-low noise digital synthesizer generates syntonized system clocks
- Multiple coherent syntonized clocks are utilized to support ethernet transceivers and measurement
- PTP timestamps are maintain internally with respect to the syntonized clocks and the phase correction can be added independently for concurrent operation of different clock domains (for example counter rotating clock rings)
- This enables support of concurrent clock domains and features such as multi-domain high accuracy topologies with enhanced resiliency

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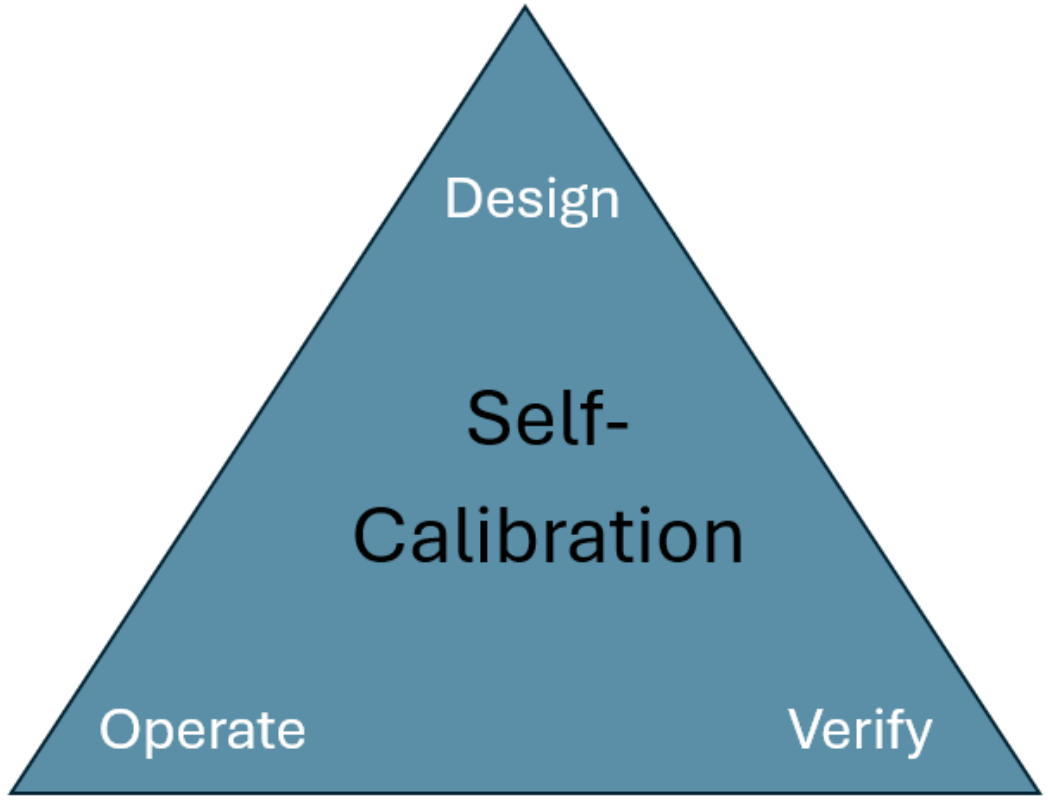
Self-Calibration Principles

- Measurements are only as good as delay calibration
- Design: delays constrained by intentionally good design
- Operate: certain delays (e.g. transceiver) are prone to modal behavior which can be suppressed with proper operation
- Verify: delay paths are verified with internal (FGPA) techniques such as loopback and word alignment



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Carrier Phase compared to Time Stamp Measurement

- **Carrier phase measurement**
  - Complements timestamp measurement in much the same way that carrier phase measurement complements code delay measurement in GNSS systems
- **Timestamp measurement**
  - Standard accuracy PTP utilizes event timestamping
  - Limited The timestamp is an isolated event which limits resolution to the single shot performance of the time to digital converter TDC
  - Even so timestamp measurement is now achieving nanosecond performance with well designed TDC and self-calibration

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Carrier Phase Measurement “Unparallel Stability”

- **Carrier phase measurement**
  - Observed over a window of time associated with the timestamp events
  - Carrier phase is cyclical which can be leverage to obtain a phase measurement with orders of magnitude less uncertainty than with the timestamp measurements
- **Novel measurement approach utilized and interrogation approach that is controlled by parameters in software to achieve optimal performance over the full range of optical loss in a real network**

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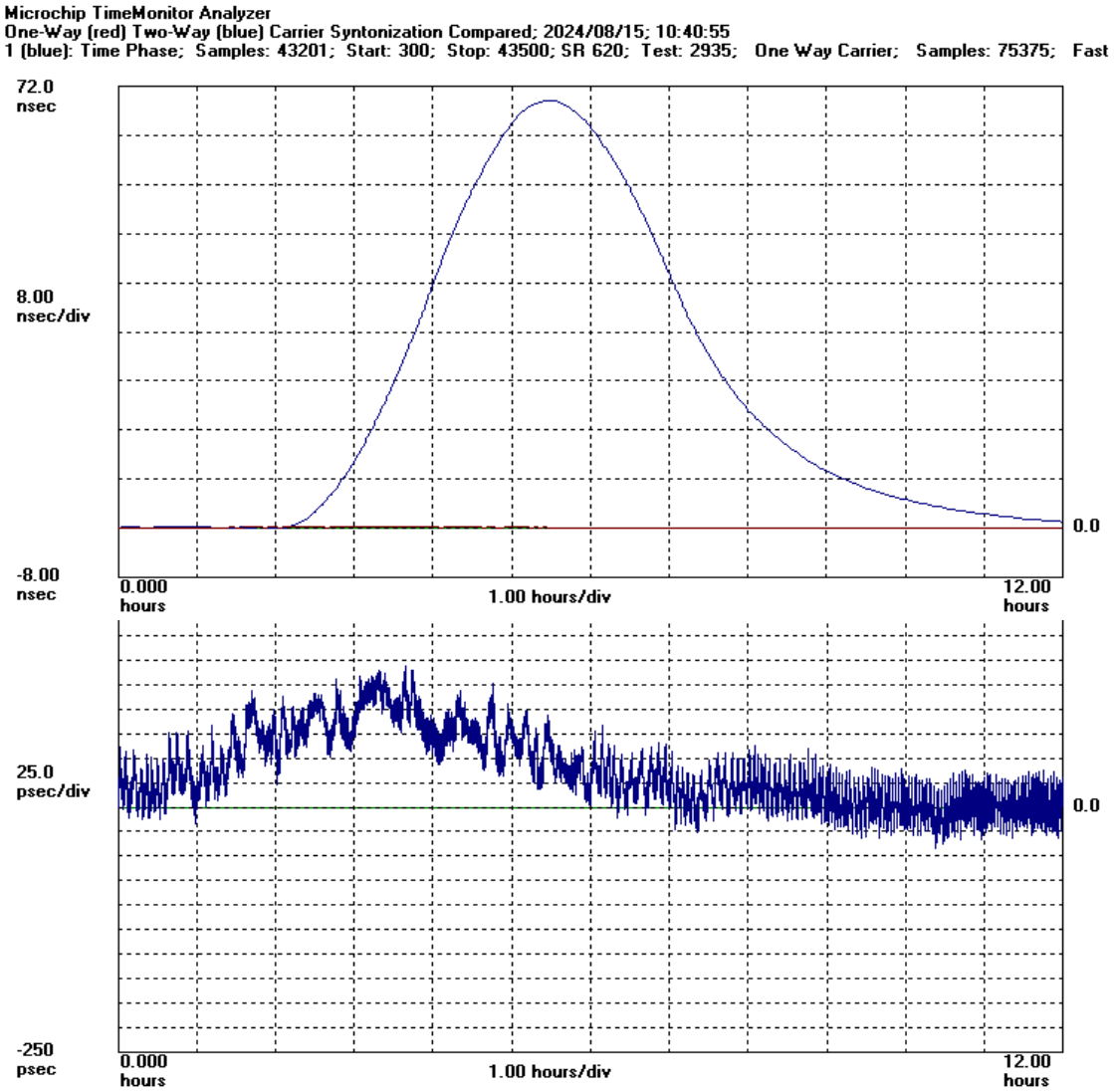
Two-Way Carrier Phase (Actual Performance)

- Two TP4500 (In Oven at 25C)
- 100km fiber (In Oven 25C to 50C)
- Remote carrier measurements transferred on PTP link at 8Hz.
- One-way (blue) show 70ns variation
- Second graph zooms in on two-way performance



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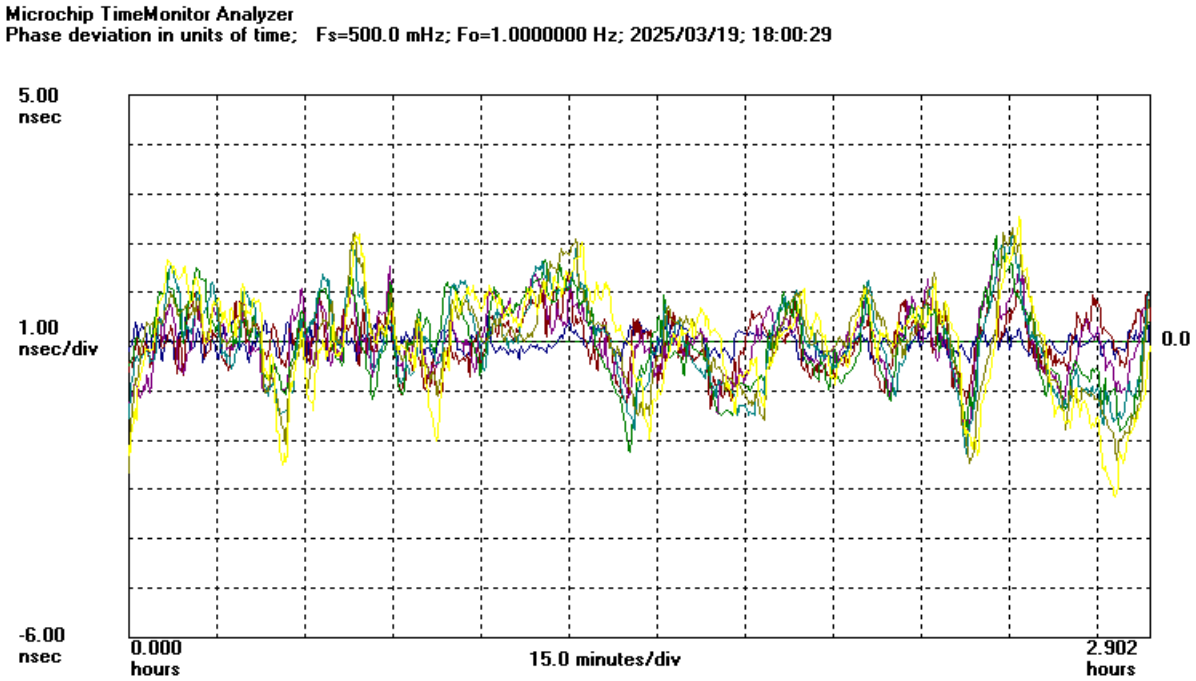
Chain of Clocks with Self-Calibration but no Carrier Phase

- Chain of seven TimeProvider® 4500 clocks
- Operating with standard G8275.1 protocol
- Performance at nanosecond level over entire chain
- No carrier phase enhancement needed



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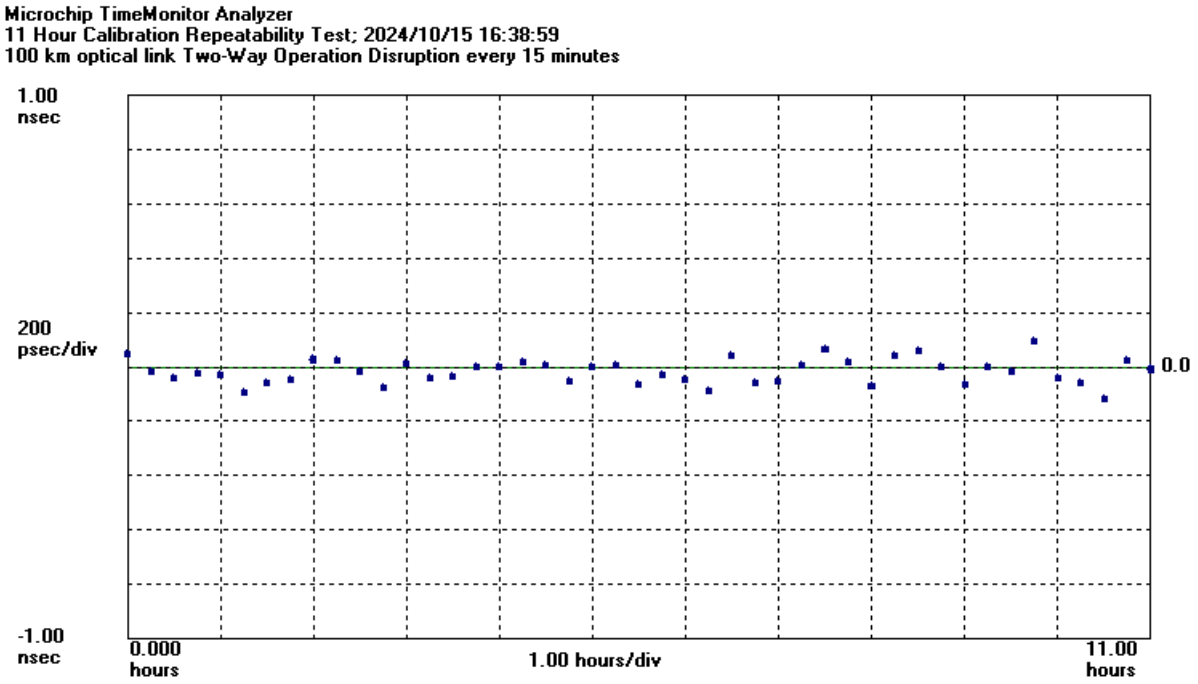
Self Calibration Repeatability Overnight “Fiber Cuts”

- Two TP4500 units
- 100 km fiber (on bench)
- Fiber cuts every 15 minutes
- Calibration repeatability better than 50ps (one sigma)



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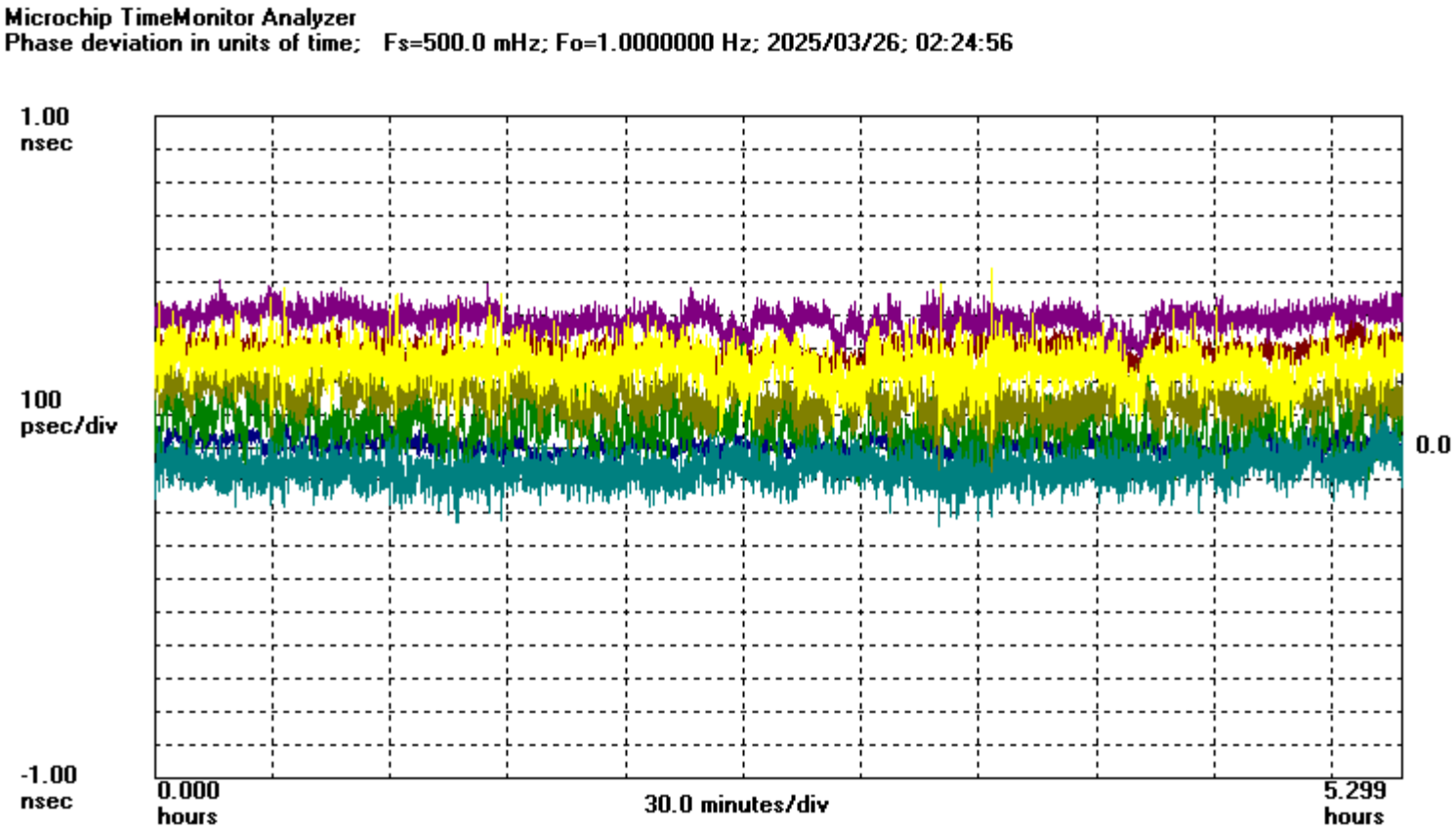
Chain of Clocks with Self-Calibration and Carrier Phase

- Seven TP4500 clocks in chain
- Datacenter use case (fiber links less than 20km)
- Stability under 100ps throughout chain
- Self-Calibration well within 1 ns



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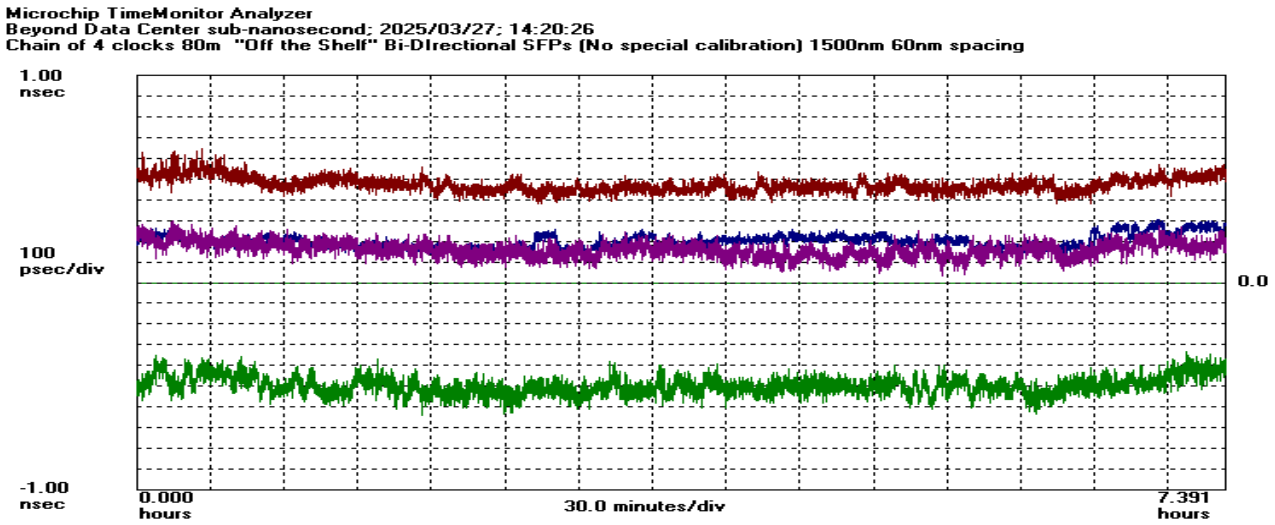
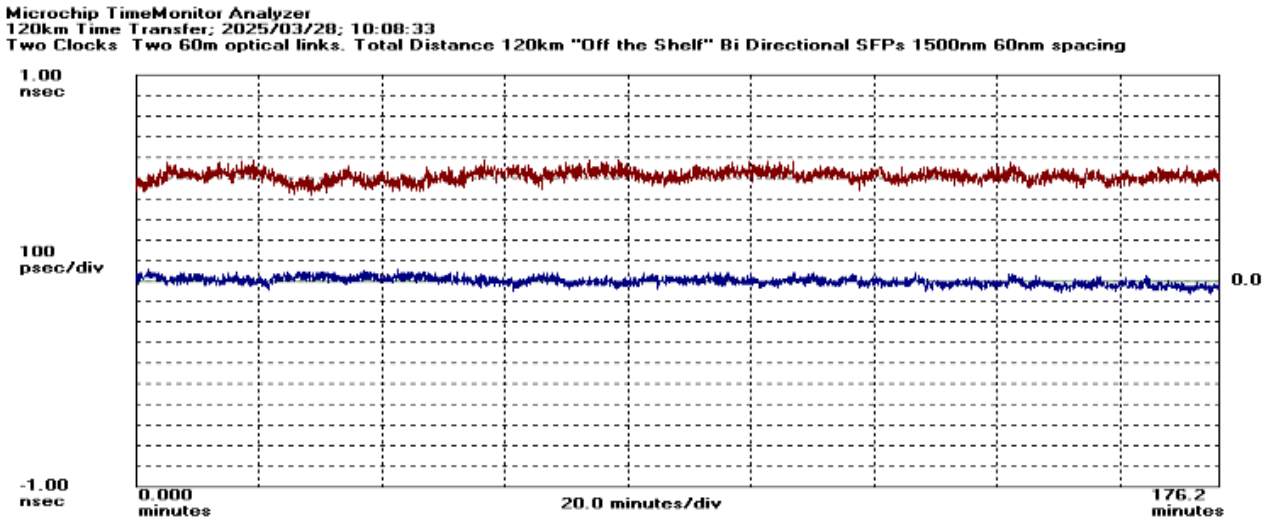
Chain of Clocks Beyond Data Center range

- **First graph**
  - 4 clocks spaced 20km apart (80km range)
- **Second graph**
  - 2 clocks space 60km apart (120km range)
- **Both achieve <u>sub-nanosecond</u> performance**
- **Off-the-shelf Bidirectional SFPs with no calibration used**





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Conclusions

- **High Accuracy does not require a revolution but an orderly evolution**
  - PTP networks can continue to use mature proven PTP protocols and tools
  - Agnostic design will also support next generation PTP protocols as needed (for example high capacity “PTP reflector”)
  - Self-Calibration achieves nano-second level repeatable performance without the use of carrier phase enhancement
  - Stability is greatly enhanced with carrier phase, but overall time transfer limited by calibration uncertainty to sub-nanosecond

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