

Getting in Sync with Open Source Addressing RAN Requirements

Workshop on Synchronization and Timing Systems

March 14th, 2023

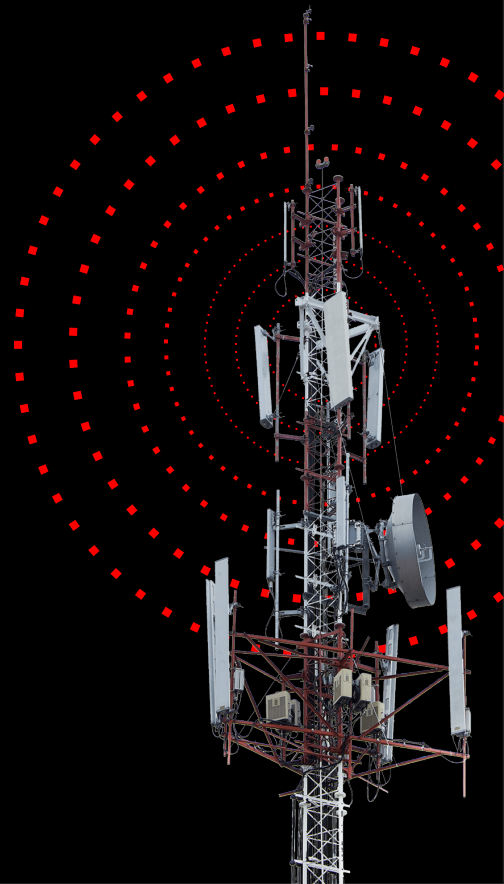
Vancouver, Canada

WSTS

Pasi Vaananen

Systems Architect, Office of the CTO

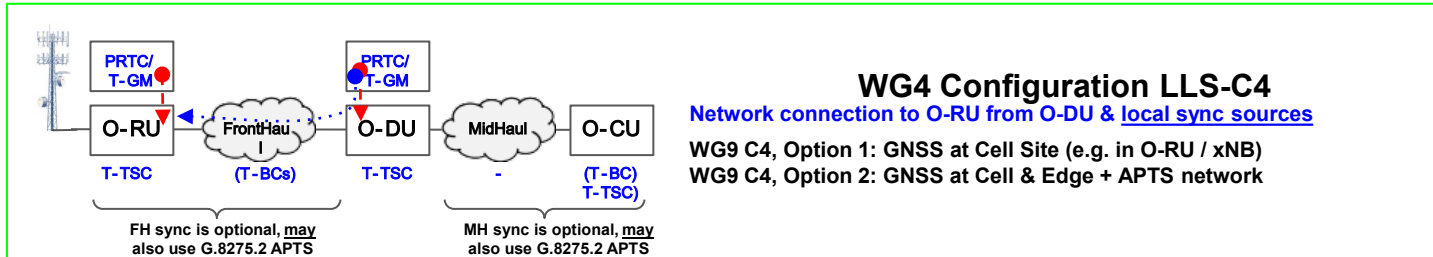
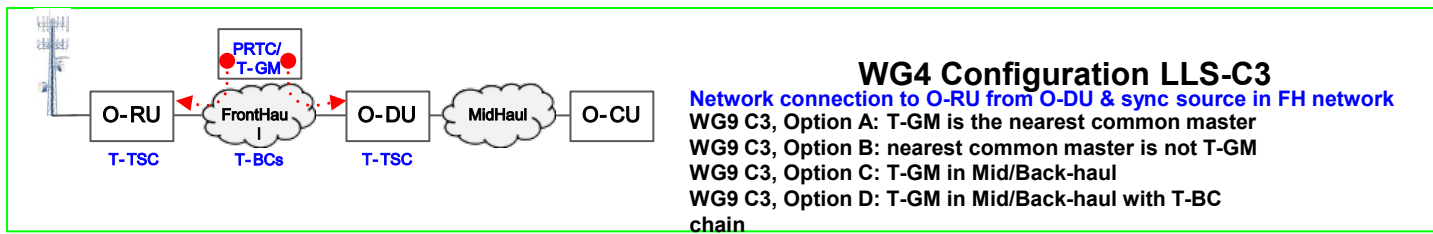
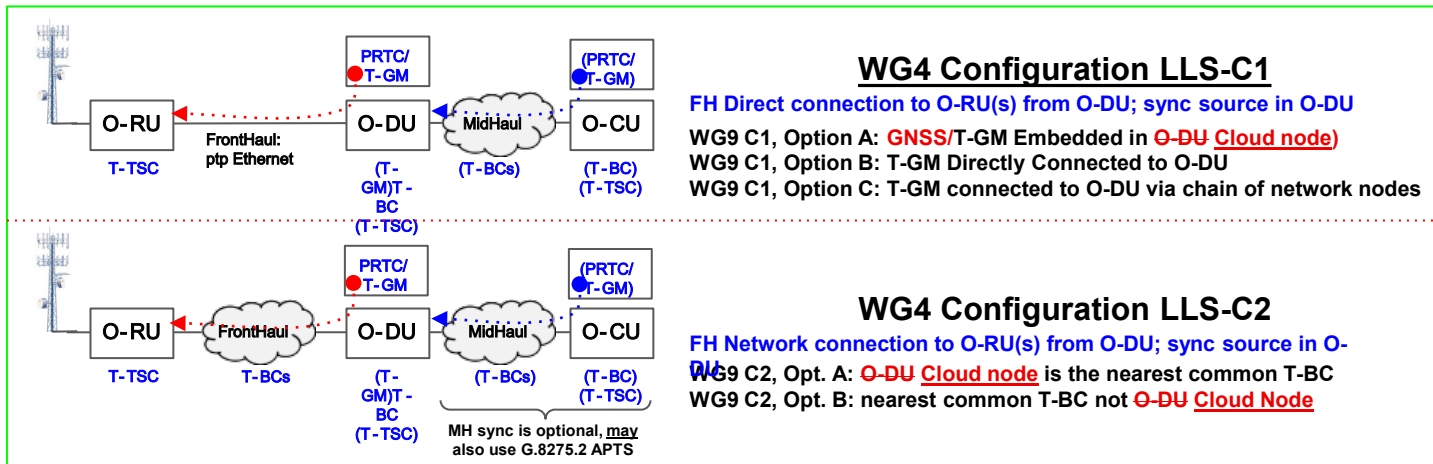
Telco Enablement & Solutions



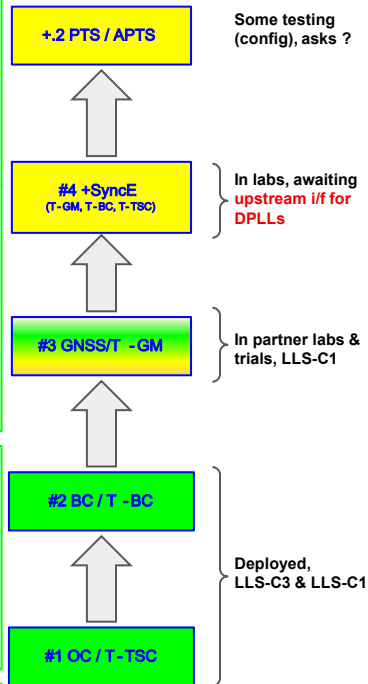
Agenda

- (O-)RAN synchronization network topologies and clock types
- Server node synchronization HW & SW implementation
- ITU-T Performance requirements summary
- Our Test Environment & Capabilities Overview
- Test results examples for different clock types
- Impact of SyncE on time/phase Synchronization performance

O-RAN “LLS-Cx” vs. Target Clock Types



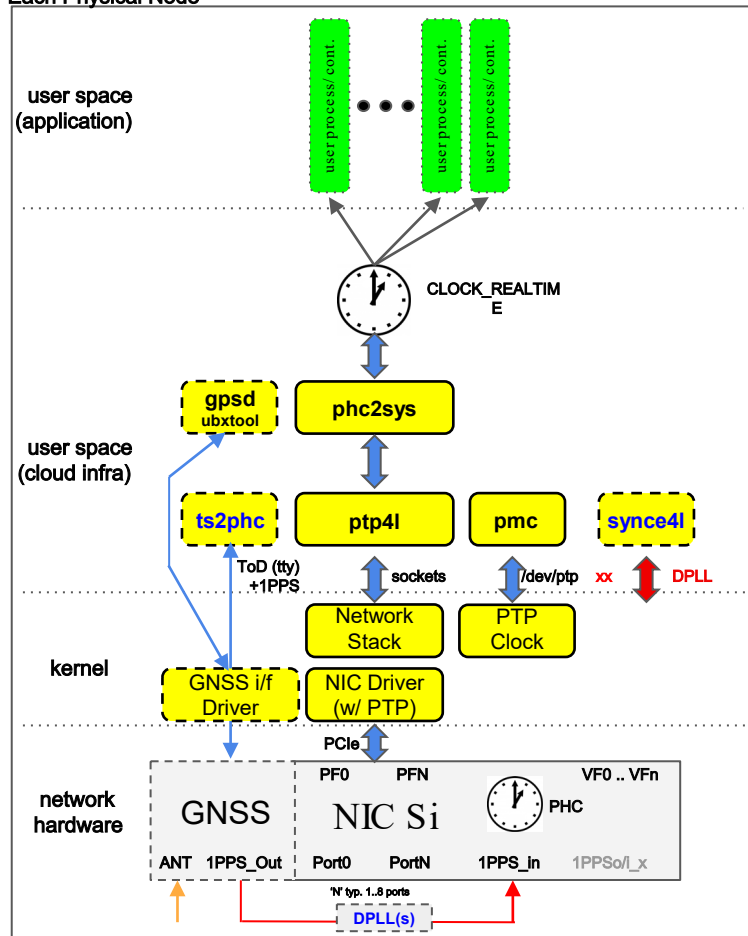
(O-)RAN Market priority list



Note:
 In clouds, synchronization is part of cloud infrastructure, and decoupled from RAN instances

Synchronization Components in Linux / k8s nodes

Each Physical Node



Key Components of the node Synchronization implementations

- HW specific synchronization SW support features are implemented in HW device drivers
- HW Clock (PHC) support in NIC Si is required for high accuracy; SyncE requires DPLLs
- **Linuxptp** is an Open Source project implementation of the PTP SW stack for Linux
- **ptp4l** implements Boundary Clock (BC) and Ordinary Clock (OC), it synchronizes PTP hardware clock (PHC) to remote master clock
- ptp4l is very flexible, and can be configured to support specific profiles, assuming that HW & driver supports associated features (e.g. PHC, L3 vs. L2 transport, accuracy targets)
- **phc2sys** synchronizes two or more clocks in the system, typically used to synchronize the system clock from PTP / PHC
- **pmc** - PTP management client; 1588 basic management access for ptp4l
- **ts2phc** synchronizes PHC(s) from external reference signals, such as 1PPS_in and ToD messages- used in multi-card T-BC, and GNSS driven T-GM configurations
- **synce4l** : implements ESMC protocol and associated state transition controls
- **gpsd/ubxtool** can be used to interface w/ GNSS receivers / u-blox specifics for configuration management and status monitoring
- In k8s clusters, synchronization functions are configured and monitored with k8s, and associated general CM, PM and FM event and metrics tools.
- O-RAN WG6 specifies a notification interface to inform synchronization users about node synchronization state changes



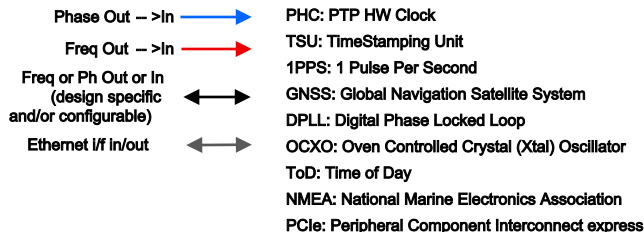
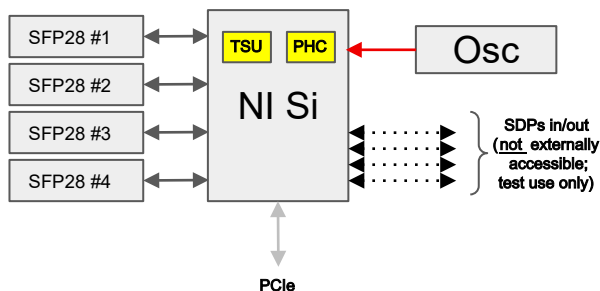
And many other
Si & HW Partners



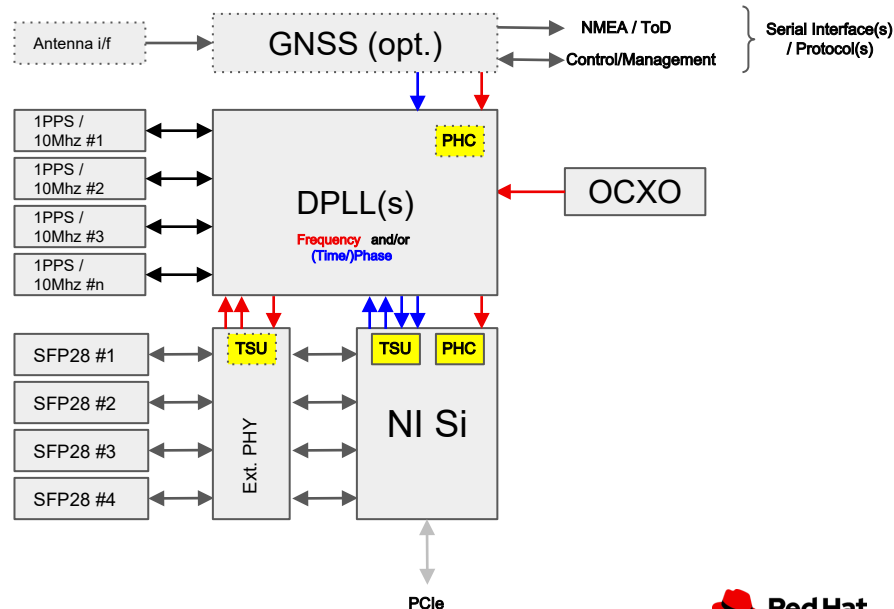
2 kinds of typical HW from Sync. & SW Perspective

- Synchronization optimized designs add various functions, typically DPLL and PHY clock recovery/generation, as well as phase/freq physical inputs and outputs, and GNSS options all which need SW enablement for configuration, monitoring and control purposes
- Various design specific ways to achieve equivalent things, none is “right” or “wrong”, they are just different; goal is to abstract to the “right” level through Linux interfaces and device drivers
- FPGA cards and SoCs with embedded NI functionality are generally similar in design from sync perspective (i.e. incorporate “NI Si” block below)

“Basic” PTP HW-timestamping capable HW Without Synchronization Enhancements Features



HW With Synchronization Enhancements Features



The Test applicability - non-SyncE and SyncE capable HW

Test Cases	Basic HW	Enhanced HW (w/ SyncE)
G.8273.2 7.1.x: TE Noise Generation	Yes, all; 7.1.4.x TE _R defined for Class-C only	
G.8273.2 7.2.x: Noise Tolerance	Yes 7.2.1 (A/B) vs. 7.2.2 (C)	Yes, 7.2.2 (Class C)
G.8273.2 7.3.x: Noise Transfer	7.3.1 PTP-PTP only	Yes, 7.3.1 PTP-PTP & 7.3.3 phy. layer freq to PTP (C/D)
G.8273.2 7.4.1 Transient Response	(7.4.1.2 PTP only; perf is FFS)	Yes
G.8273.2 7.4.2 Holdover Performance	(7.4.2.1 PTP only; perf is FFS)	Yes; Class-C mask FFS

- We do also conduct the applicable tests for 1PPS and/or 10Mhz phase/freq. Reference outputs if those outputs are supported as physical interface with connectors
- In “standard” cards without connectorization, we may also use these for testing if available e.g. through pin headers, but they are expected to **not** be used/usable/supported in end-application
- Also, G.8262.1 eEEEC test sequence typically applies to SyncE capable cards, not shown here
- We view eEEEC tests more of DVT tests, minimum SW impact; primarily FW/driver/DPLL configs

G.8273.2 T-TSC & T-BC Noise Gen Reqs Summary

Parameter	Class-A	Class-B	Class-C	(Class-D); Still WIP in ITU-T	Notes
7.1 Max. Absolute Time Error; $\max TE $	≤ 100 ns	≤ 70 ns	≤ 30 ns	(≤ 15 ns)	Unfiltered measurement, absolute value
7.1 Max. Absolute Time Error; $\max TE_L $	-	-	-	≤ 5 ns	0.1Hz low-pass filtered, 1000s measurement, absolute value
7.1.1 Max. Constant Time Error; cTE	$\leq \pm 50$ ns	$\leq \pm 20$ ns	$\leq \pm 10$ ns	($\leq \pm 4$ ns)	cTE Averaged over 1000s
7.1.2 Max. dynamic Time Error, 0.1Hz Low-Pass Filtered; dTE_L (MTIE)	≤ 40 ns		≤ 10 ns	(≤ 3 ns)	MTIE Mask, 1000s observation interval constant temp., (10000s for A/B variable temp.)
7.1.2 Max. dynamic Time Error, 0.1Hz Low-Pass Filtered; dTE_L (TDEV)	4 ns		2 ns	(≤ 1 ns)	TDEV Mask, 1000s observation interval at constant temp.
7.1.3 Max. dynamic Time Error, 0.1Hz High Pass Filtered; dTE_H	70 ns p-p		FFS (30ns p-p?)	(15 ns p-p)	Peak-to-peak value, 1000s measurement
7.1.4.1 Relative constant Time Error Noise Generation; cTE_R	FFS		$\leq \pm 12$ ns	FFS	cTE averaged over 1000s
7.1.4.2 Relative dynamic Time Error Low-Pass Filtered Noise Generation; dTE_{RL} (MTIE)	FFS		≤ 14 ns	FFS	MTIE Mask; 1000s observation interval at constant temp.

7 **Note:** Accuracy required is primarily determined by specific Use Case requirements & number of elements on the synchronization transfer path

Synchronization Test Setup at Red Hat TelcoLab

Path -delay calibrated
Optical single -mode Switch
for remote/automated test
reconfiguration

Spirent TestCenter for Bulk
Traffic testing ($\leq 1.2\text{Tbps}$)

Spirent TC for Detailed Perf.
Testing ($\leq 800\text{Gbps}$), w/
PTP/SyncE slave emulation

Calnex Attero - 100G
Network Emulation System

Calnex Paragon Neo
PTP/SyncE analyzer w/
comprehensive SW feature
set for Telco PTP & SyncE

Keysight 8ch Scope w/
time&freq analysis SW

Cisco&Dell PTP/SyncE capable
Switches & routers (back)

Primary GNSS signal splitters
(roof antenna + simulator)

1PPS & 10Mhz reference
distribution amplifiers

Primary ePRTC (TP4100 +
5071A w/ hi -performance CBT)

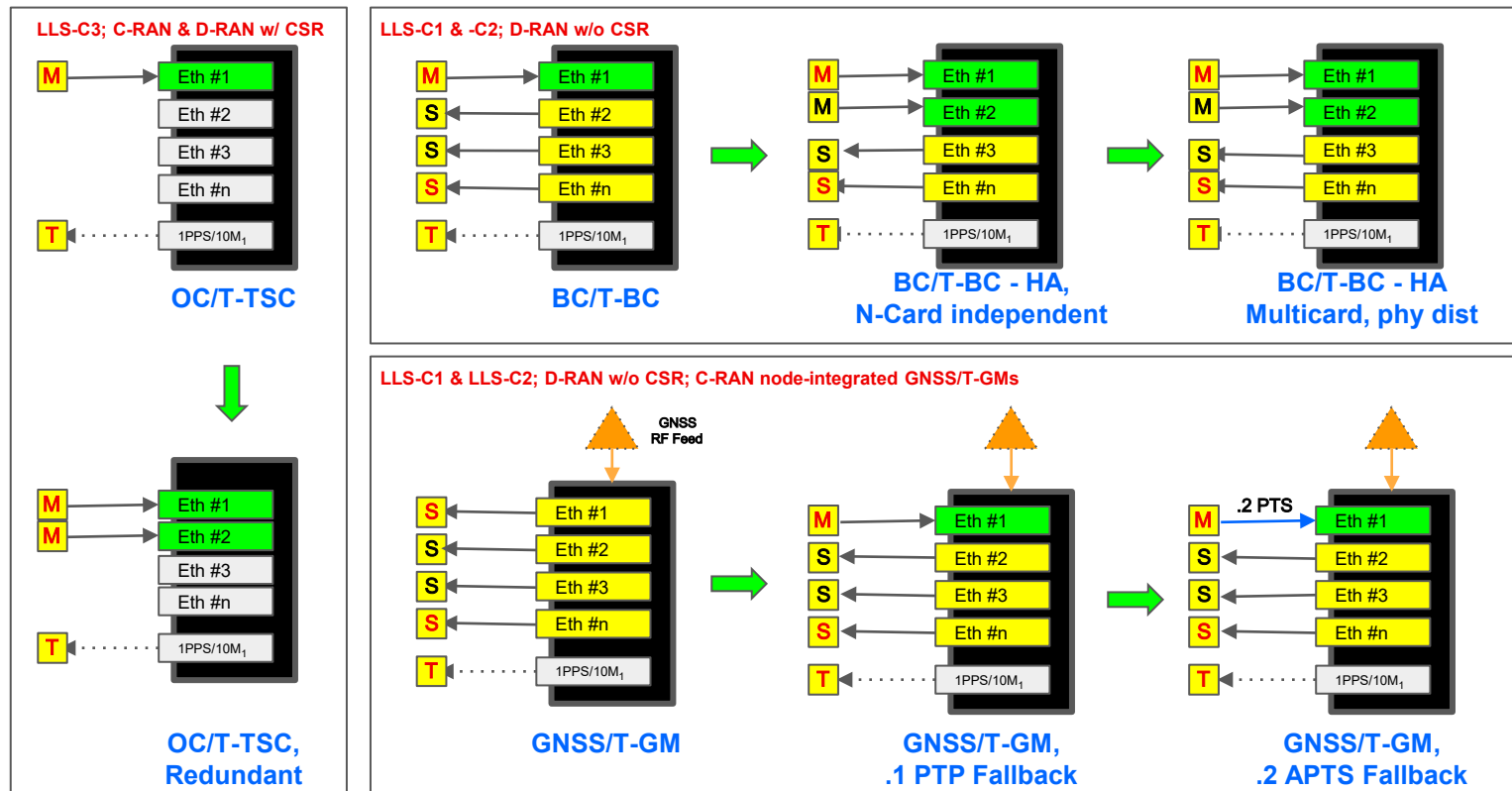
Secondary ePRTC (TP4100 +
5071A w/ hi -performance CBT)

Spirent GNSS Constellation
Simulation System

22x servers w/ various NICs,
FPGA, SoC etc. PCIe cards w/
Sync. Support ("DUT" servers)

1PPS/10M signal switch (rear)

Test Target Adjacencies for Black-Box DUTs Overview



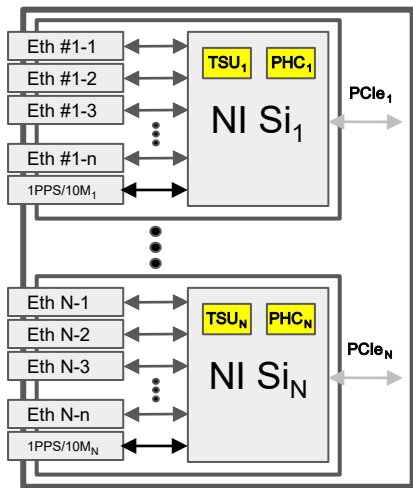
- G.8275.1 FTS (+opt SyncE subject to HW support); M → S
- G.8275.2 PTS (+opt SyncE) can be substituted to any i/f
- G.8275.1 PTS (+ opt optional SyncE subject to HW support); M → S
- 1PPS | 10Mhz test signal, if supported by HW; as needed (opt.)

- M** PTP (+optionally SyncE) Master Port; external to DUT
- S** PTP (+optionally SyncE) Slave Port; external to DUT
- T** 1PPS or 10Mhz Test input port; external to DUT; optional

Red **M/S/T** main test ports

Server DUTs as “Grey Boxes”, multi-card (simplified)

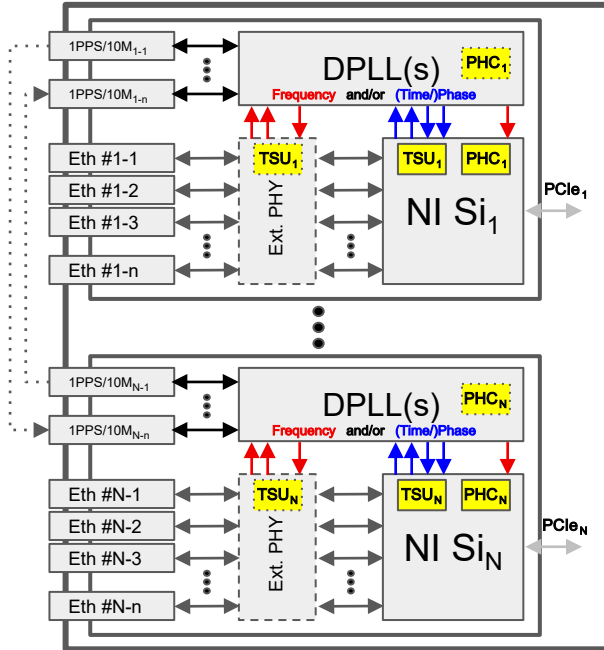
OC/BC (1..N “basic” NICs)



OC/BC, Target Configurations:

- Up to N*n PTP Interfaces
- OC: typ 1 or 2 (HA, 1 or 2-card) active i/f's
- BC: typ N*(1*slave + n*1*Master)
- OC: 1*ptp4l + 1*phc2sys
- BC: N*ptp4l + 1*phc2sys
- 1PPS/10M: out only, lab / field test

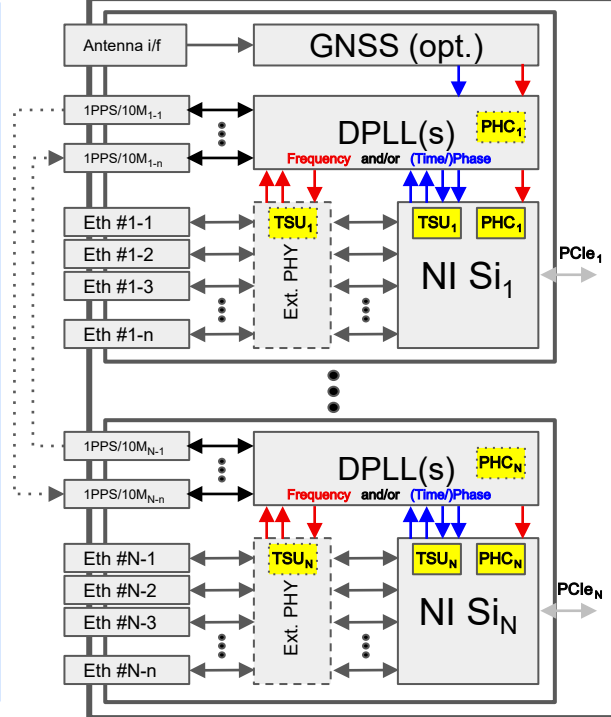
T-TSC/T-BC (1..N “enhanced” NICs)



T-TSC/T -BC, Target Configurations:

- Up to N*n PTP Interfaces
- T-TSC: typ 1..2 (HA, 1 or 2-card) active i/f's
- T-BC: typ N*(1*slave + n*1*Master) i/f's, possibly less slaves than cards when cards synchronized w/ physical signals
- T-TSC: 1*ptp4l + 1*phc2sys + 1*sync4l
- T-BC: 1..N*ptp4l + 1*phc2sys + 1*ts2phc + 1*sync4l
- 1PPS/10Mhz monitoring (out) + in (multicard sync with physical signals, using ts2phc to sync PHCs)

GNSS/T-GM (1..N “enhanced” NICs)



GNSS/T -GM Target Configurations:

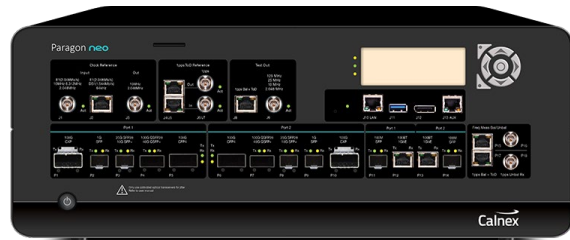
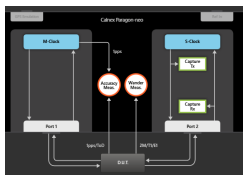
- Basics as with T-TSC/T -BC
- Plus 1xGNSS (using ts2phc, different config)
- +gpsd and/or +ubxtool, dep. on use case
- T-GM: up to N*n Master i/f's

Set-up for a G.8275.1&G.8273.2 T-BC (T-TSC) w/ Neo

Cs Frequency Standard (+ ePRTC)



10Mhz
(opt. 1PPS+ToD)

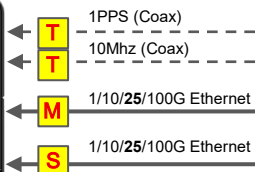


Paragon Neo PTP Tester

Notes:

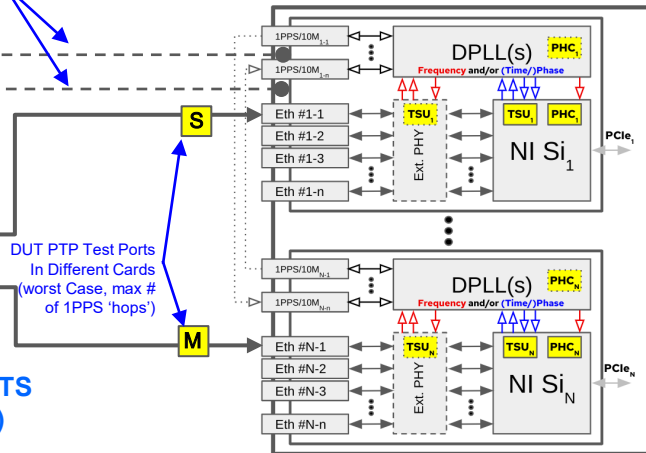
- Only a single port-pair + 1PPS & 10Mhz can be measured at the time
- Measurement of the System Clock (i.e. OS / CPU clock) is not possible in normal CPU SKUs, and those that have some time enabled pins are not commonly used
- No under-load testing, or if enabled only port pair, not sufficient to exercise entire NIC and/or PCIe related issues (latter is esp. relevant to phc2sys / time transfer over PCIe)

Physical 1PPS and/or 10Mhz,
as supported / required



G.8275.1 PTP FTS
(+SyncE opt.)

DUT: T-BC w/ N cards (2 shown)



OC/T-TSC Clock Tests:

- OC/T-TSC configuration is subset, at least one Neo Master to at least one DUT Slave port
- OC/T-TSC tests require measurement signal back to tested, i.e. 1PPS
- In Practice, if it meets specific class as (T-)BC, it will do at least as well as T-TSC/OC, and (T-)BC test does not mandate need for 1PPS physical signals

Using the Linux / PTP metrics and events

TEST EXECUTION

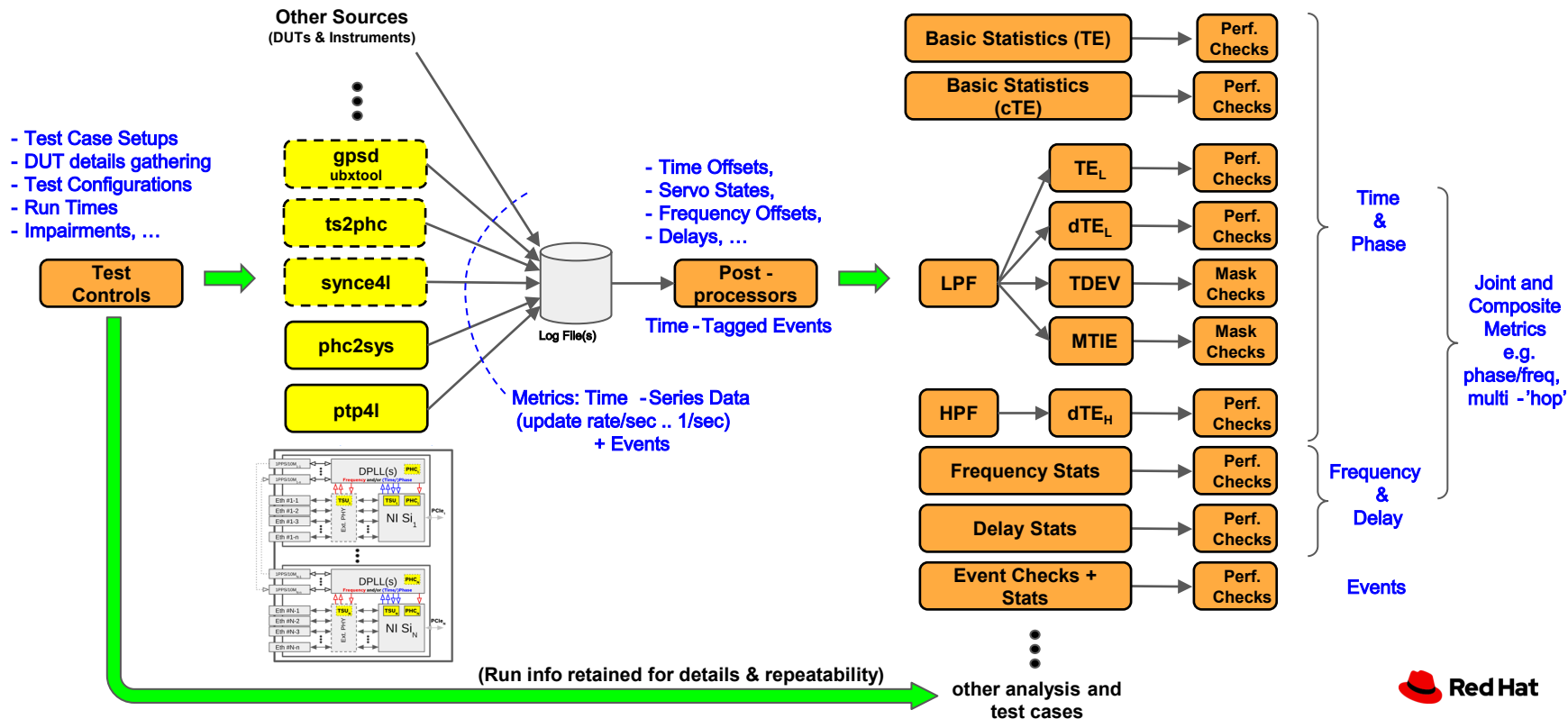
For Each Node and
Each Test-Run Sequence

DATA COLLECTION

For Each Node in Test Configuration,
and each synchronizer / clock pair

DATA ANALYSIS

Test Case Automation, Compliance & Pass/Fail tests,
Regression Analysis, What-if Experiments...

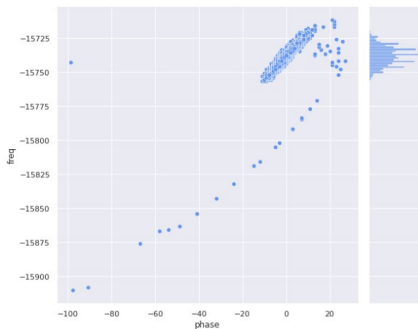


Linux / PTP metrics analysis G.8275.1, ptp4l

Basic HW

ph-freq_{INITIAL}

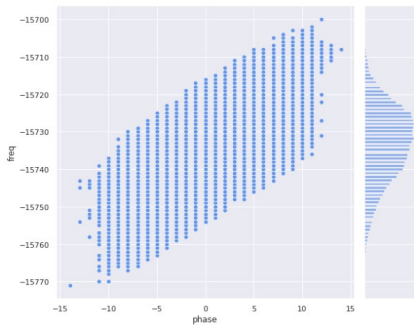
Initial Synchronization Period



Time from 1st S0 to 1st S2: 0.188 s

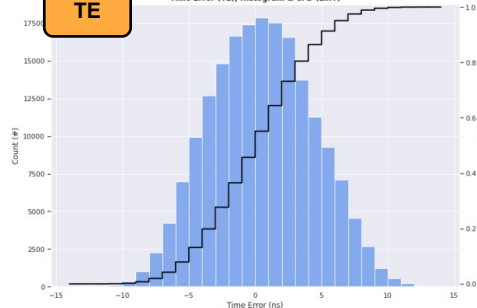
ph-freq_{INSYNC}

Initial Synchronization Period



TE

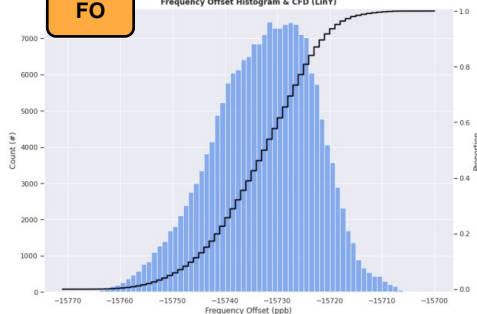
Time Error (TE), Histogram & CFD (LinY)



Min phase: -14.000 ns
Max phase: 14.000 ns
Phase stddev: 3.891 ns

FO

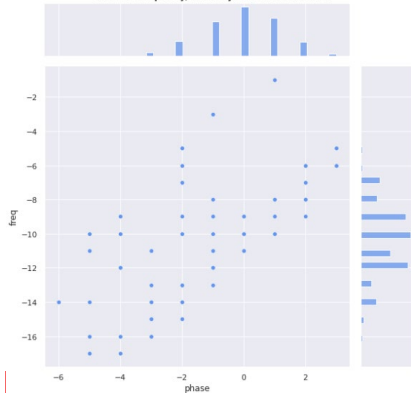
Frequency Offset Histogram & CFD (LinY)



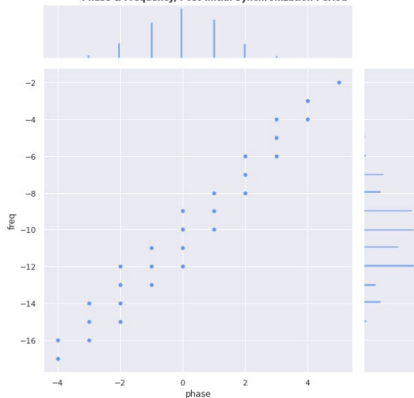
Min Freq: -15771 ppb
Max Freq: -15700 ppb
Freq stddev: 9.708 ppb

Enhanced HW; NO SyncE

Phase & Frequency, Initial Synchronization Period

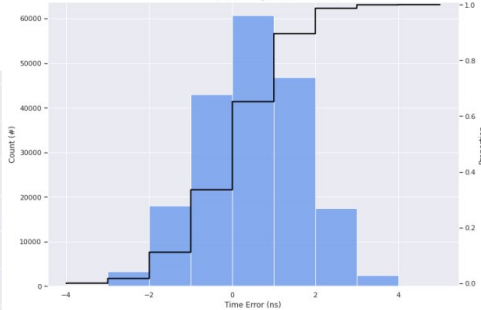


Phase & Frequency, Post-Initial Synchronization Period



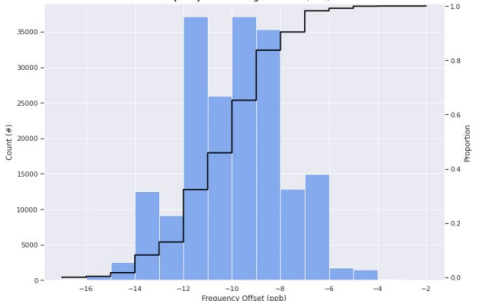
Time from 1st S0 to 1st S2: 0.251 s

Time Error (TE), Histogram & CFD (LinY)



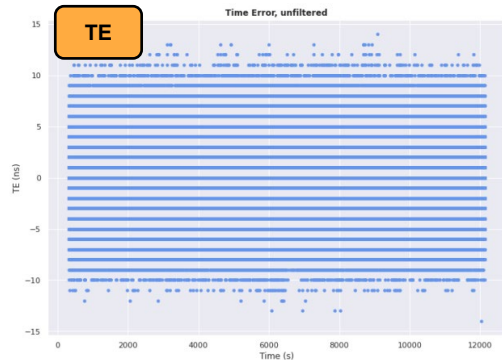
Min phase: -4.000 ns
Max phase: 5.000 ns
Phase stddev: 1.222 ns

Frequency Offset Histogram & CFD (LinY)

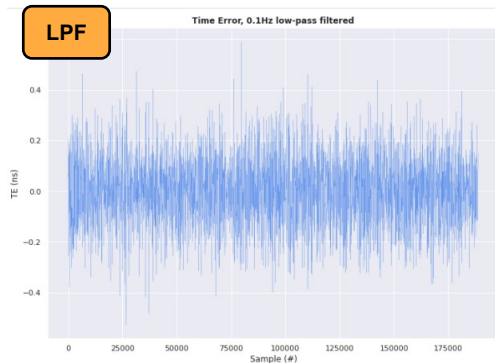


Min Freq: -17 ppb
Max Freq: -2 ppb
Freq stddev: 2.061 ppb

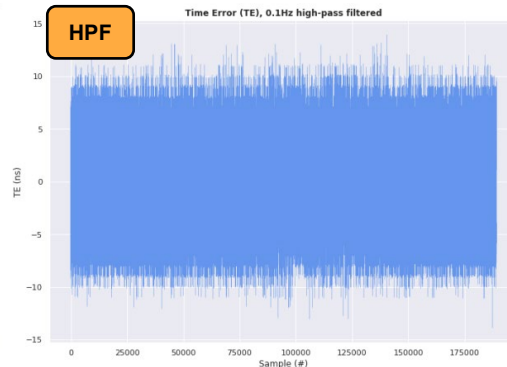
Linux / PTP metrics analysis; G.8275.1ptp41basic HW



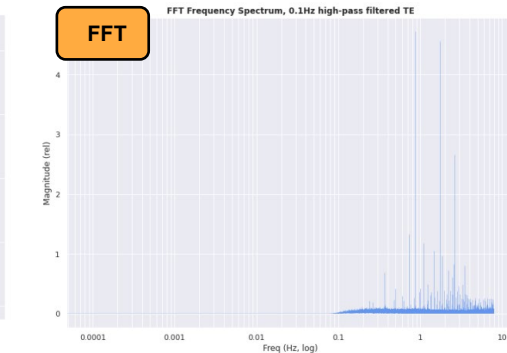
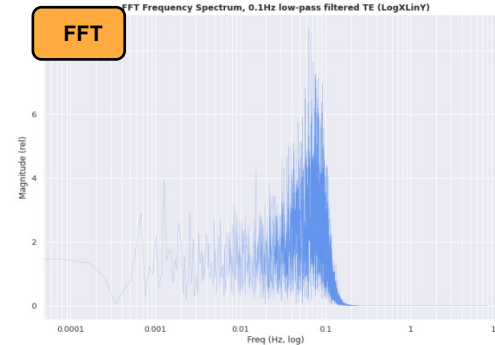
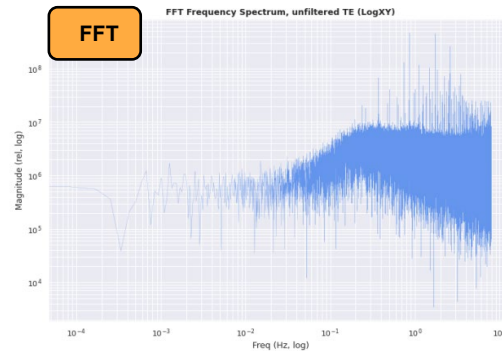
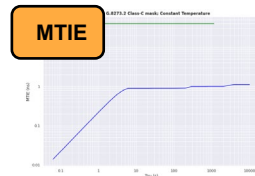
pk-pk phase: 28.000 ns
Mean phase: -0.000 ns
Min phase: -14.000 ns
Max phase: 14.000 ns
Phase stddev: 3.891 ns
Max |TE|: 14.000 ns



pk-pk lpf phase: 1.115 ns
Mean lpf phase: -0.000 ns
Min lpf phase: -0.526 ns
Max lpf phase: 0.589 ns
Lpf phase stddev: 0.127 ns
Max lpf |TE|: 0.589 ns

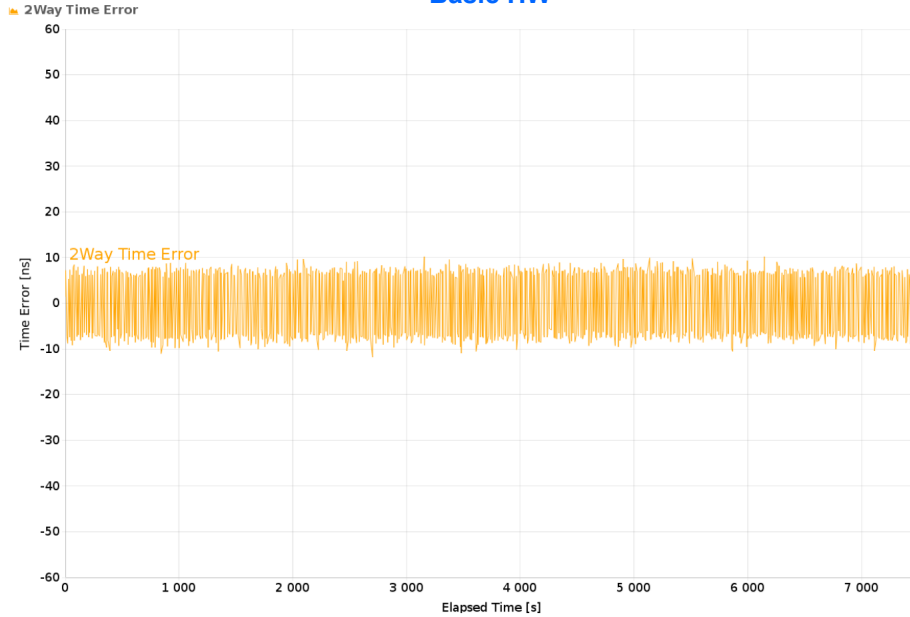


pk-pk hpf phase: 27.806 ns
Mean hpf phase: 0.000 ns
Min hpf phase: -13.900 ns
Max hpf phase: 13.905 ns
hpf phase stddev: 3.887 ns
Max hpf |TE|: 13.905 ns



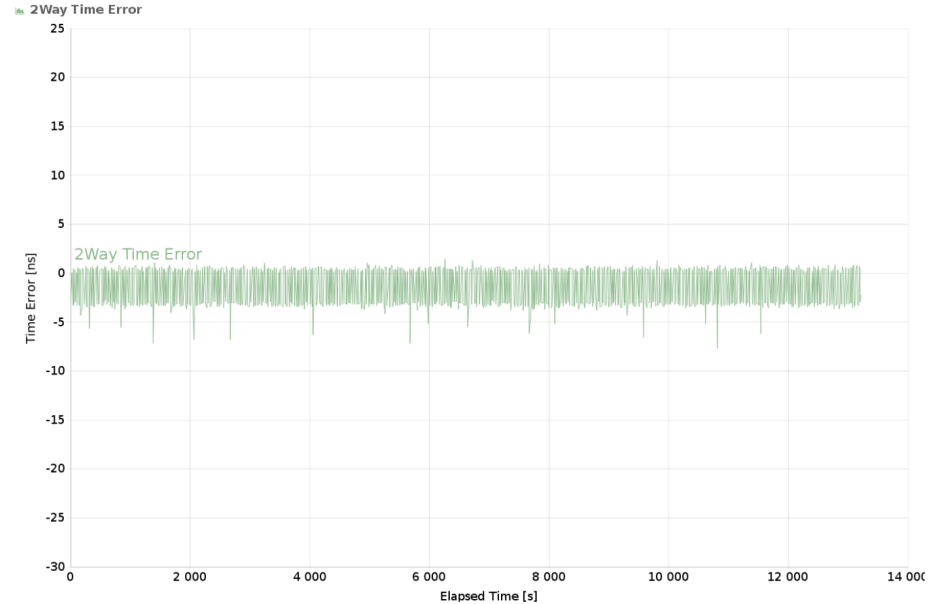
7.1T-BC Noise Generation - Unfiltered TE

Basic HW



Pk-Pk	22 ns
Mean	-0.374 ns
Min	-11.805 ns
Max	10.195 ns
Max-Min	22 ns

Enhanced HW With SyncE

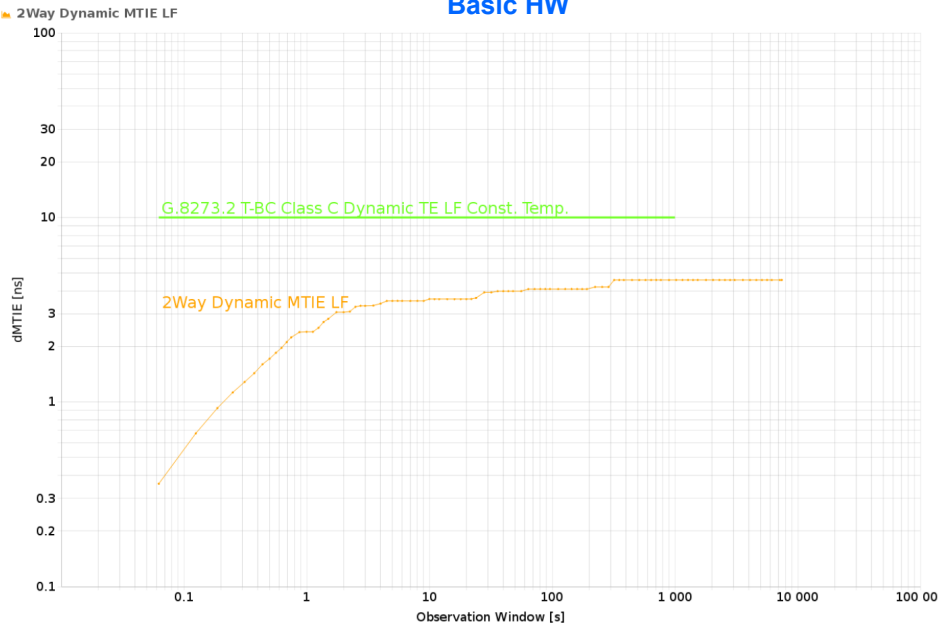


Pk-Pk	9.125 ns
Mean	-1.461 ns
Min	-7.68 ns
Max	1.445 ns
Max-Min	9.125 ns

- Both DUTs do pass Class C for TE with lots of margin (Class-C requires 30ns for Unfiltered |TE|)
- The performance with SyncE in this test is ~2x better then without it in the same configuration

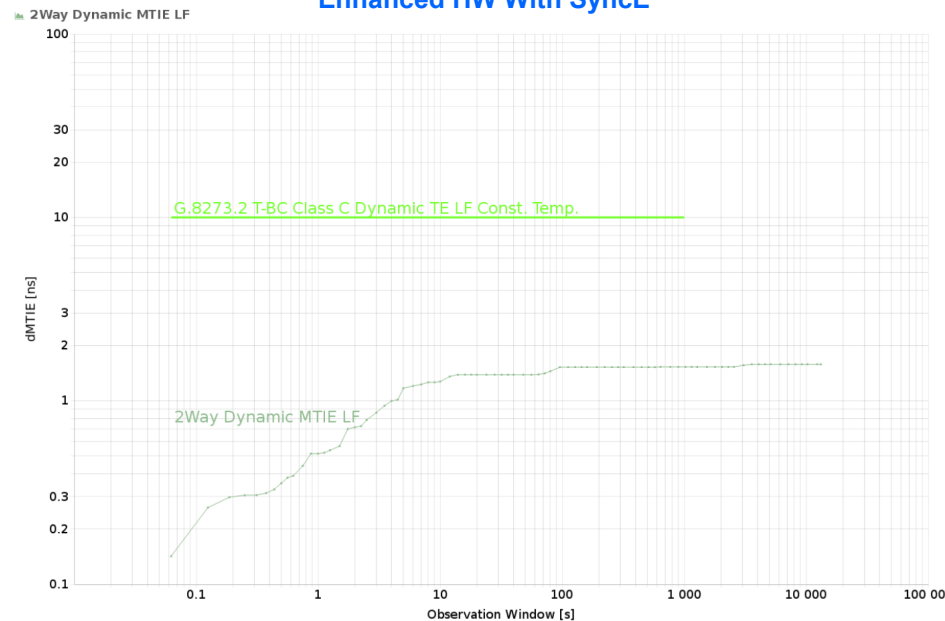
7.1.2 T-BC Noise Generation - Dyn. MTIE LF Class-C mask

Basic HW



Min	0.361 ns
Max	4.58 ns
Max-Min	4.219 ns

Enhanced HW With SyncE

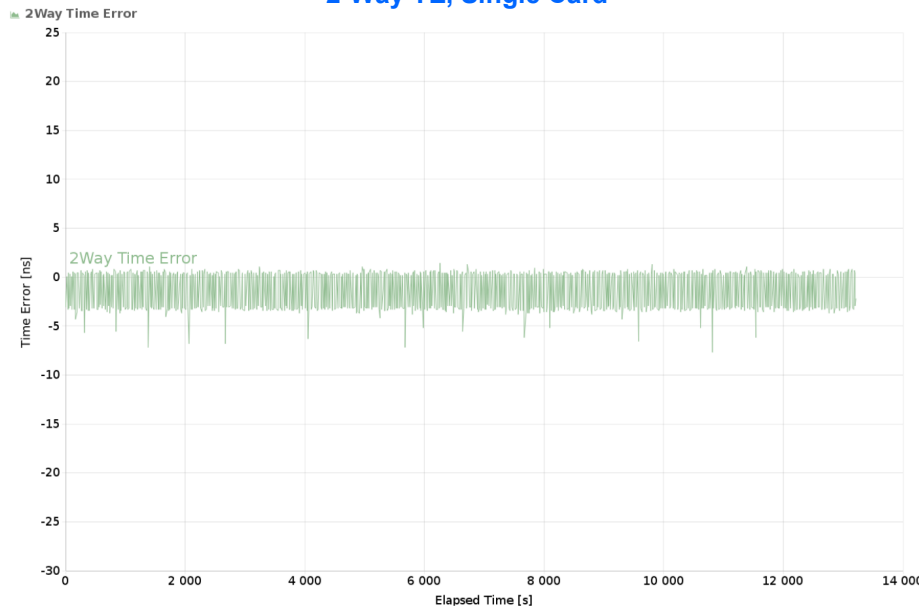


Min	0.142 ns
Max	1.582 ns
Max-Min	1.439 ns

- Both DUTs do pass Class C for MTIE LF 10ns mask (as well as TDEV mask) with margin
- The performance with SyncE in this test is >2x better then without it in the same configuration

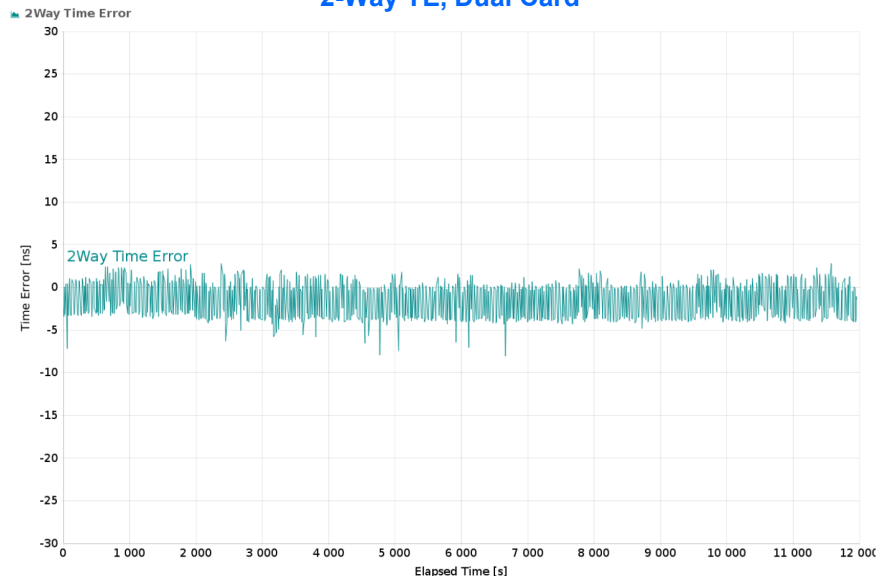
7.1T-BC Noise Generation - 1vs.2-Card with SyncE

2-Way TE, Single Card



Pk-Pk	9.125 ns
Mean	-1.461 ns
Min	-7.68 ns
Max	1.445 ns
Max-Min	9.125 ns

2-Way TE, Dual Card

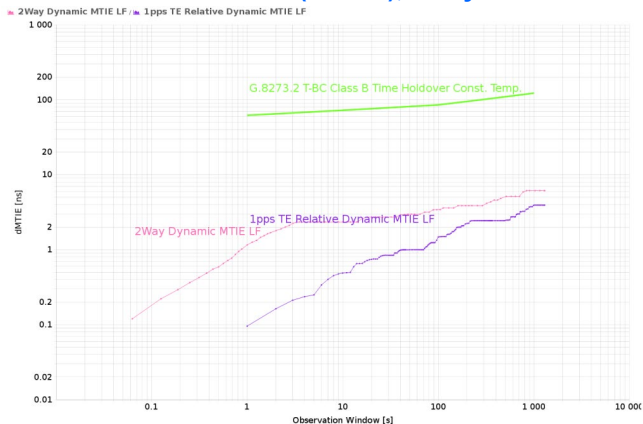


Pk-Pk	10.875 ns
Mean	-1.6 ns
Min	-8.063 ns
Max	2.812 ns
Max-Min	10.875 ns

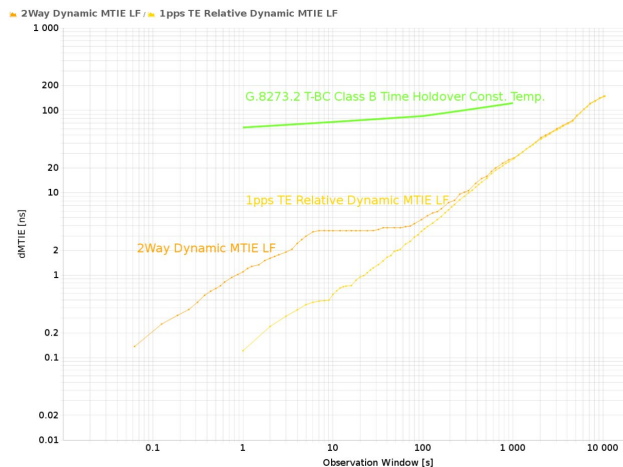
- In this test, the BC slave port is in 1st card, and master port is in 2nd card
- Combination still passes Class C for TE with margin (important, multi - card configs are common !)
- This is primarily enabled by physical phase/freq signals to sync the 2nd card from the 1st

Holdover Performance - SyncE HW (“good” OSC+DPLL)

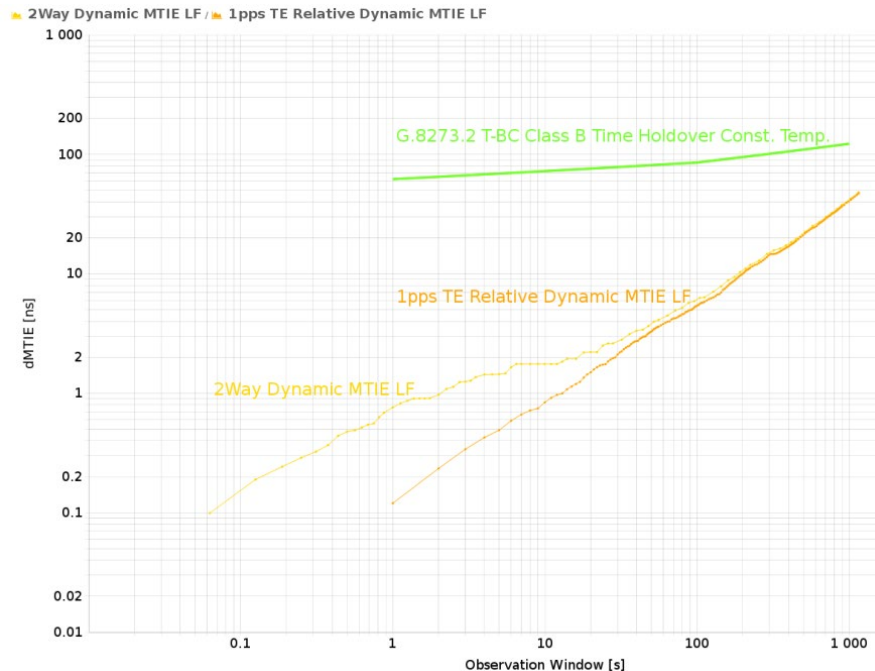
A: Holdover (dMTIE), w/ SyncE



B: Holdover (dMTIE), SyncE lost



C: Holdover (dMTIE), Freq FreeRUN - no SyncE lock/use at all



- Mask (above) is for Class-B, Class C/D is **FFS**
- ~constant temperature (lab !) tests **ONLY** done at Red Hat
- Case A: SyncE assisted holdover: ~6ns @1000sec
- Case B: SyncE lost holdover: ~25ns @1000 sec
- Case C: FreeRun, No SyncE: ~47ns @1000 sec



Get Involved & Get In Sync

Upstream projects - SW & open HW

- [Chrony](#) (primarily NTP)
- [LinuxPTP](#) project
- Linux kernel - common sync if/s
- Linux HW dev. Drivers- sync features
- OpenCompute [TAP](#)
- OpenCompute Networking
- OpenCompute Telco
- OpenCompute Telco Edge
- TIP OOPT
- TIP RAN projects
- Jupyter, Matplotlib, Scipy/Numpy, pandas, ...
- [Allantools](#)

Key Standards / Spec. Organizations

- O-RAN WG4,5,6,7,8 and 9...
- ITU [SG15 Q13/15](#)
- IEEE P802 / [802.3cx](#) (TS accuracy)
- IEEE [P1588](#)
- 3gpp

How to contact me

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Special Thanks to

- LinuxPTP community, Linux Kernel Community, our NIC Si/card & FPGA Si/card HW partners, vRAN SW partners, Calnex & Spirent & Keysight