Open Time Server and Time Card 2

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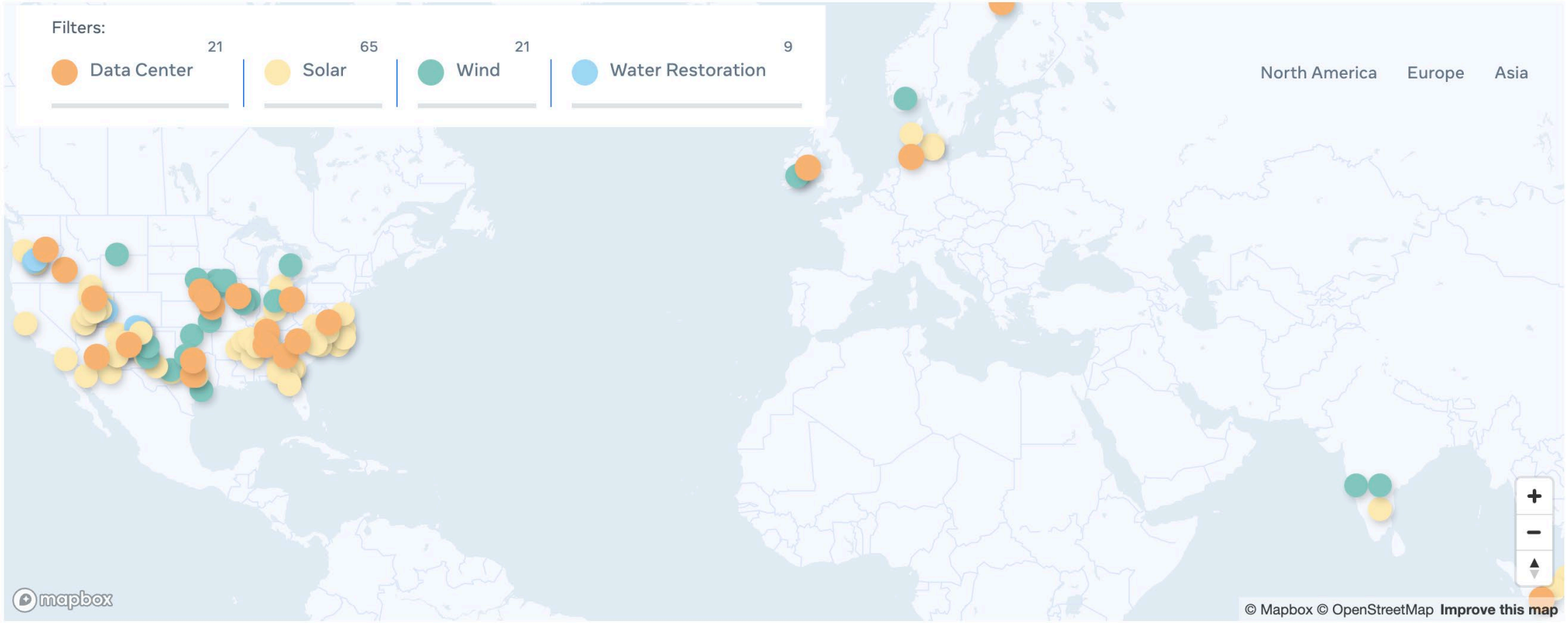
Background

Timing Architecture of a data center

- Wide and shallow
- Unicast only
- Transparent Clock only
- No 3rd party software on the data plane
- Provisioning and maintenance at scale
- Transparent and easy to assess
- Traceability

Our Global Footprint



https://datacenters.fb.com/

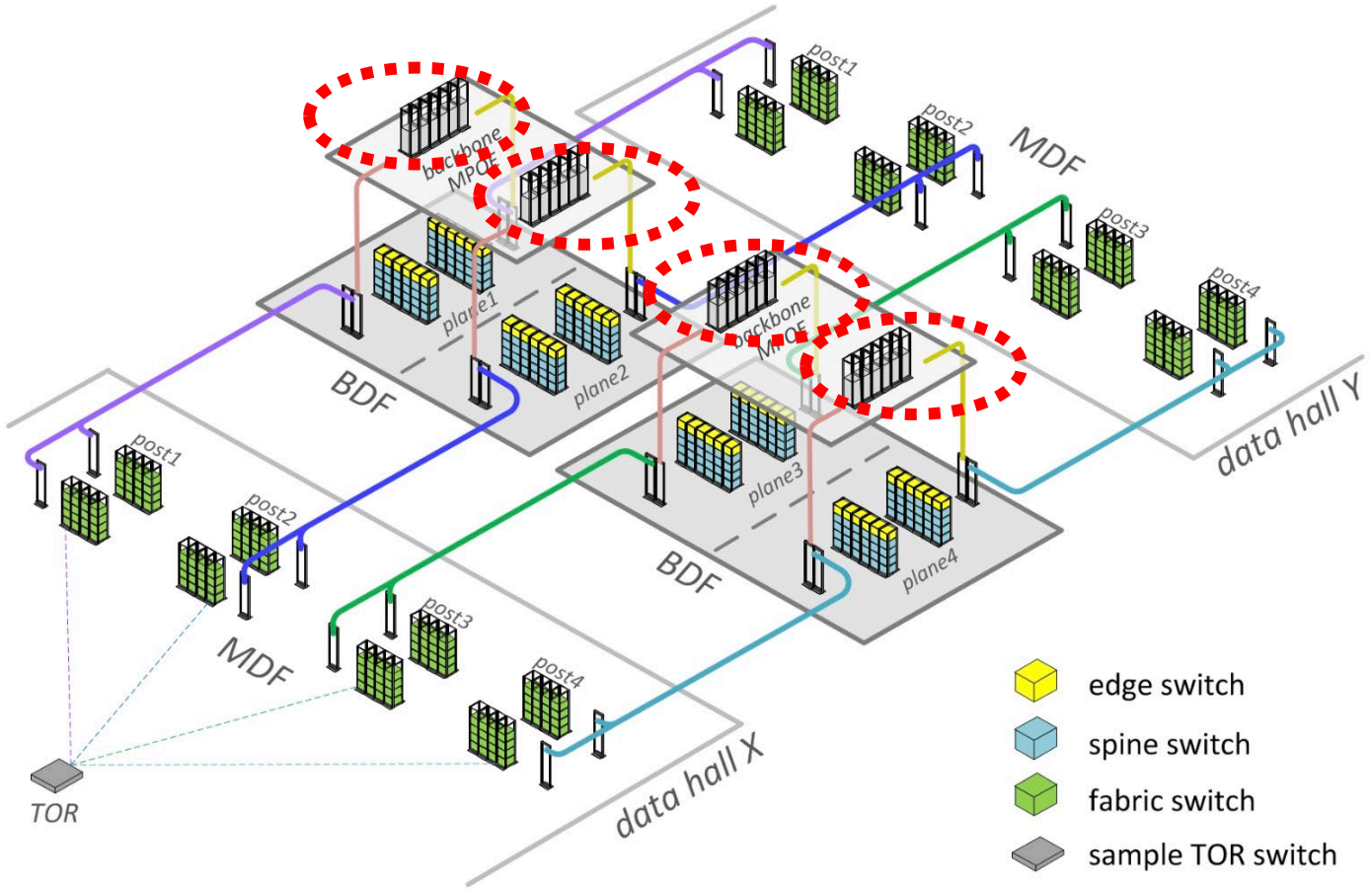
Data center and Data hall

https://www.datacenterdynamics.com/en/news/meta-to-cut-data-center-spend-says-new-ai-facilities-will-be-cheaper-faster-to-build/

What's Inside

https://www.bloomberg.com/news/articles/2017-09-25/facebook-won-t-hire-you-for-its-data-center

Data hall and Minimum Point of Entry (MPOE)



https://engineering.fb.com/2014/11/14/production-engineering/introducing-data-center-fabric-the-next-generation-facebook-data-center-network/

Towards

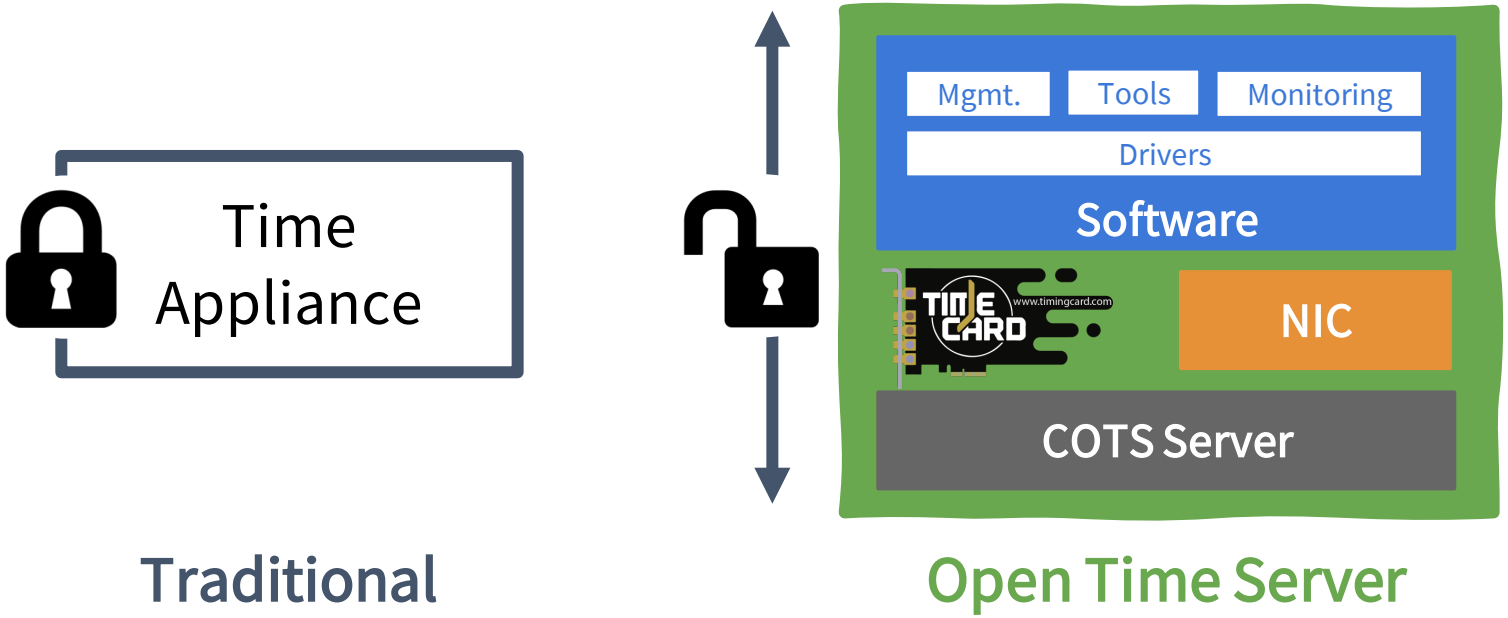
- Need for a scalable and open-source Time Server
- Feature Rich
- Flexibility
- Adaptability
- Versatility
- Backed by a community

Open Time Server

Meets all the DC requirements

- Need for a scalable and open-source Time Server
- State of the art
- Feature Rich
- Flexibility
- Adaptability

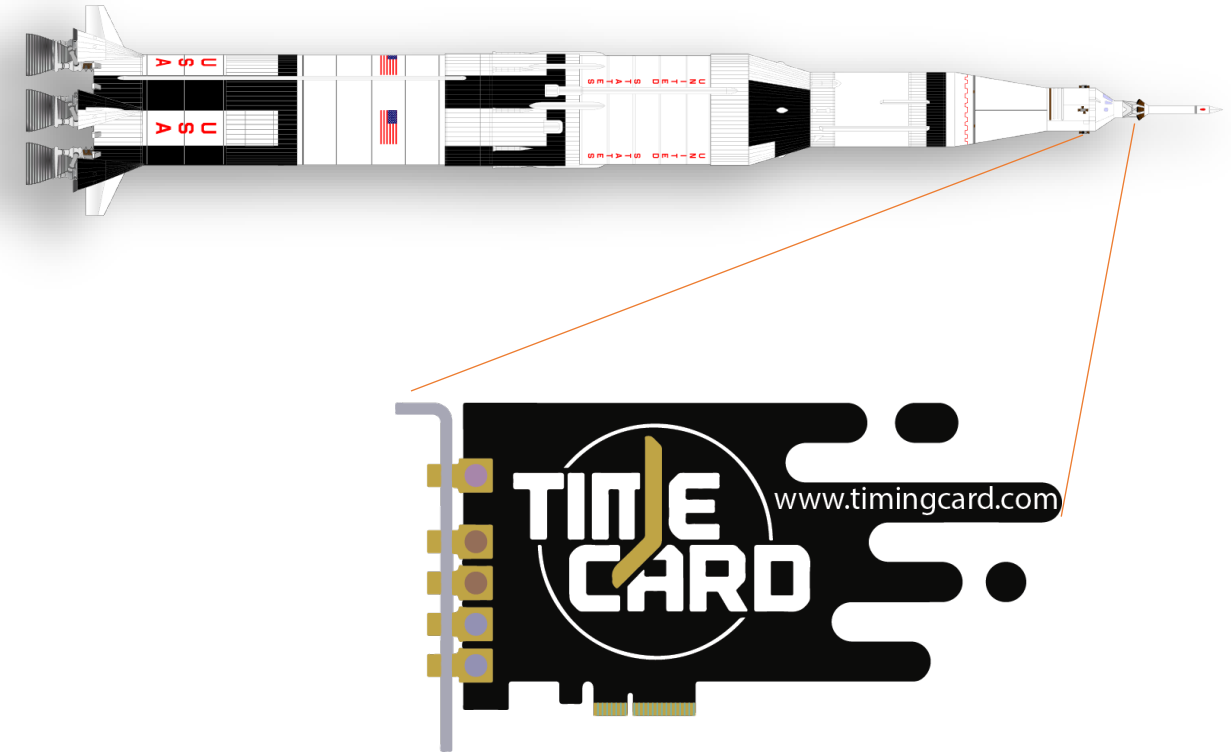
Open Time Server



At the Heart of Open Time Server: Time Card

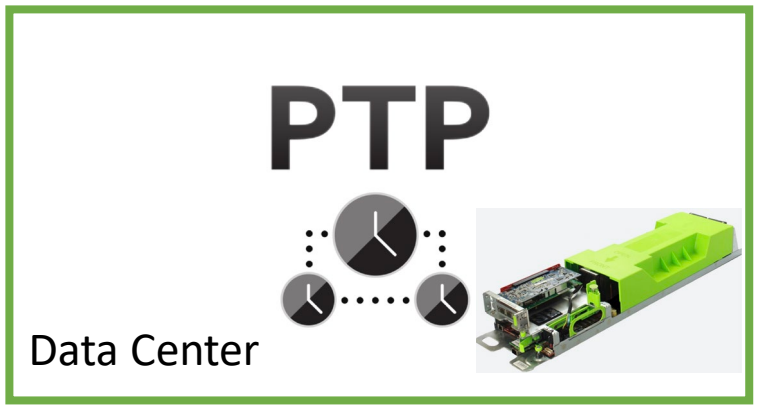
Time Keeping and Time Dissemination

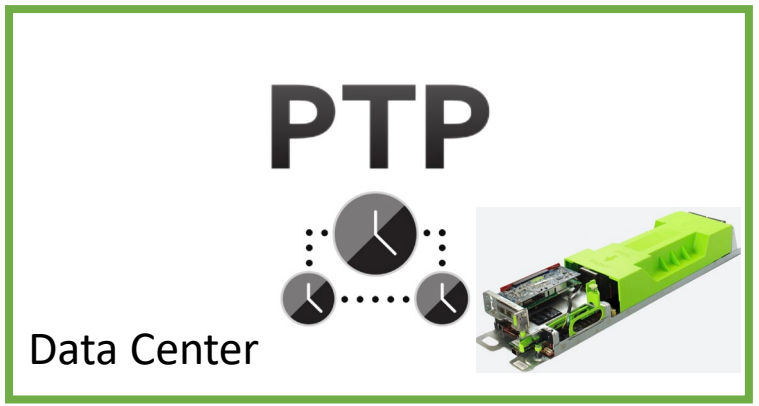
- Launch Vehicle:
  - NTP
  - PTP
  - WR
- Payload
  - Time Card (Time)



Time Sync Technologies for Different Domains

Between Data Centers



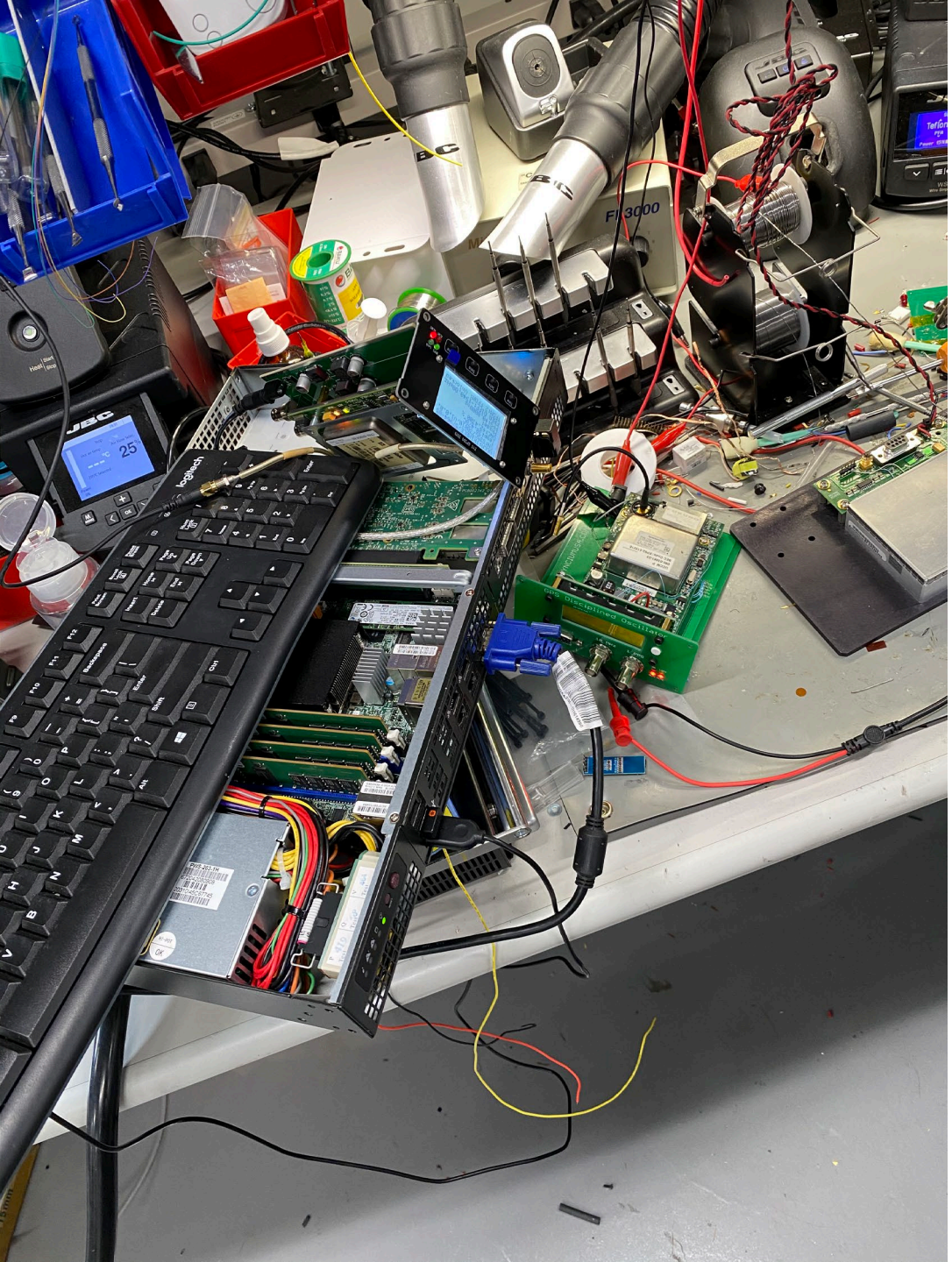


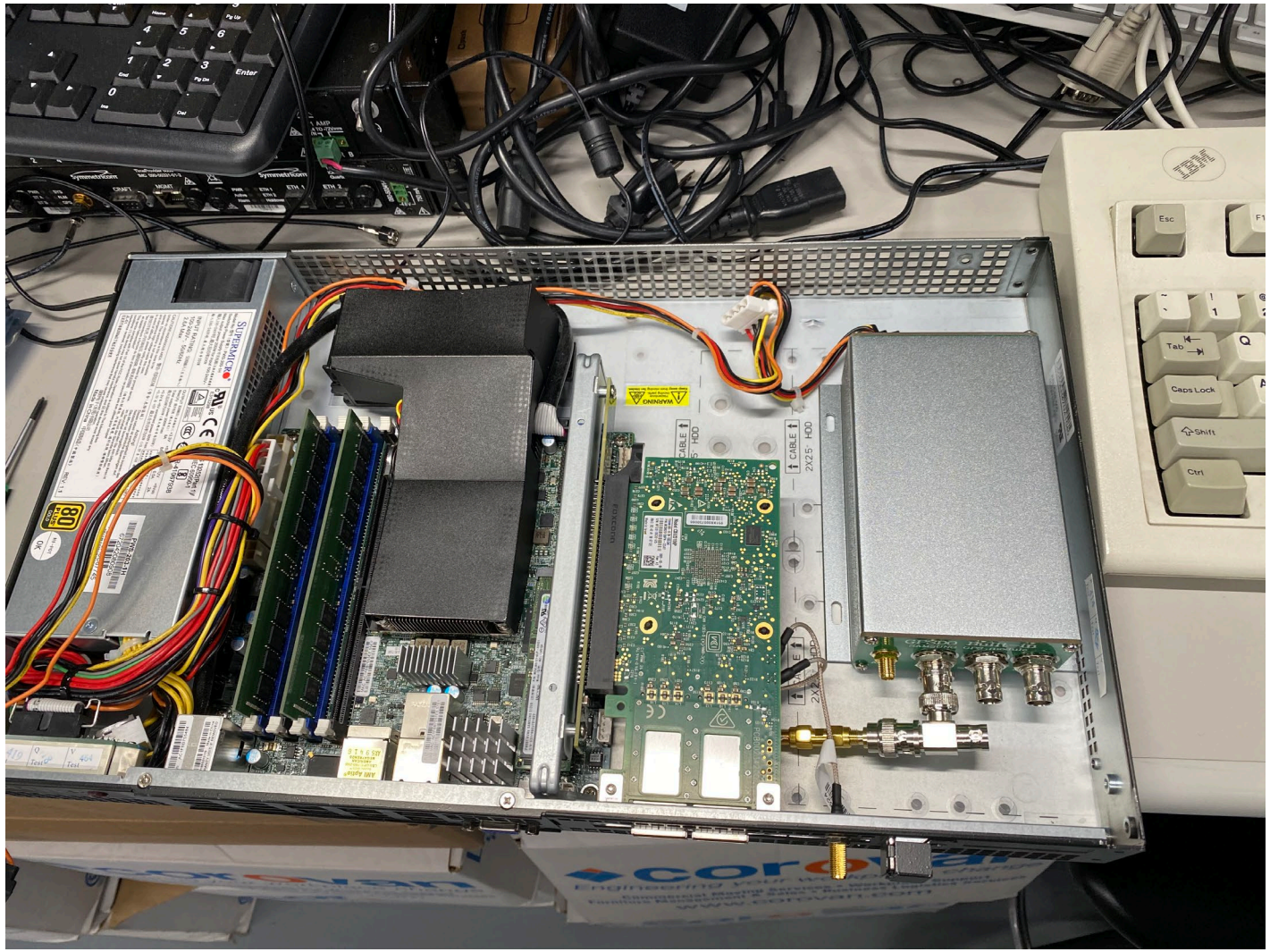
Inside Data Centers

PTM

PTM

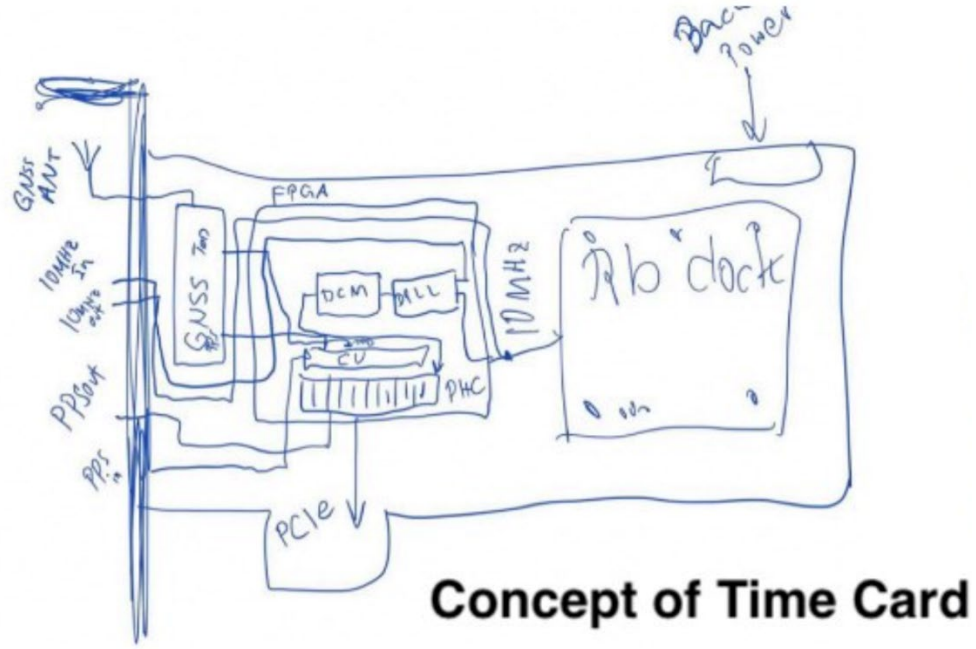
Inside Servers



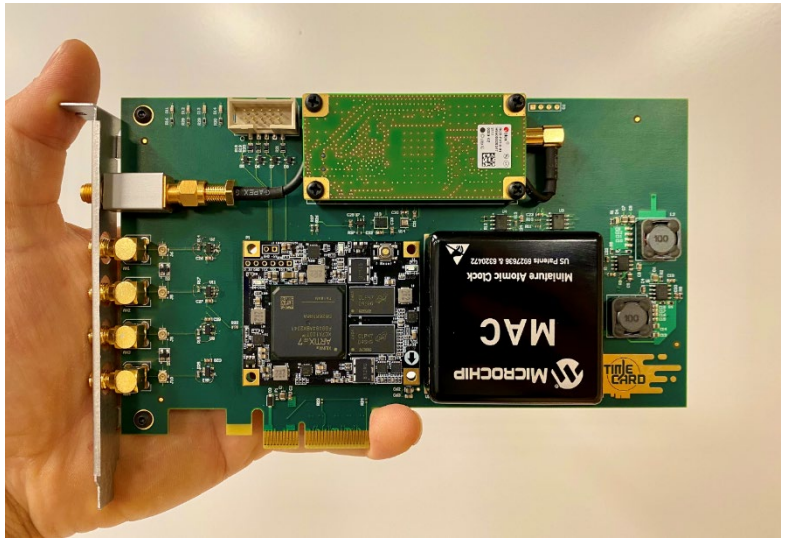


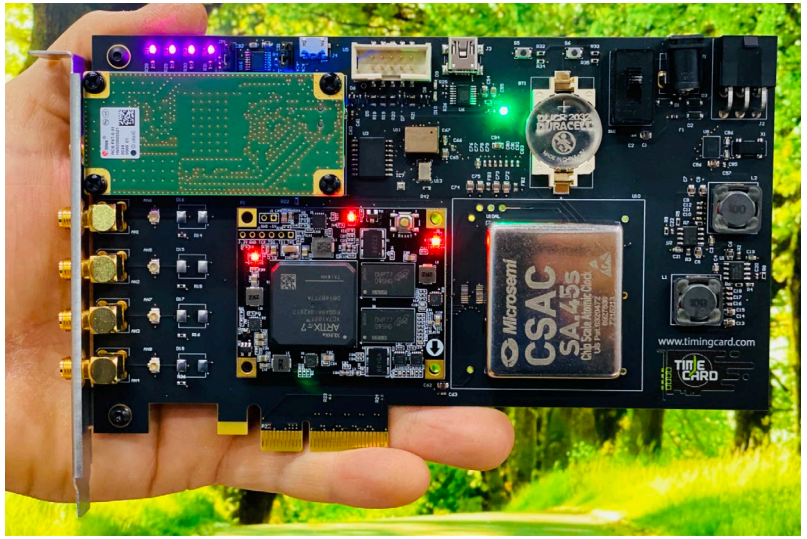
Time Card

- Concept (2020)
- First Prototype (2021)
- Industry Adoption (2022)

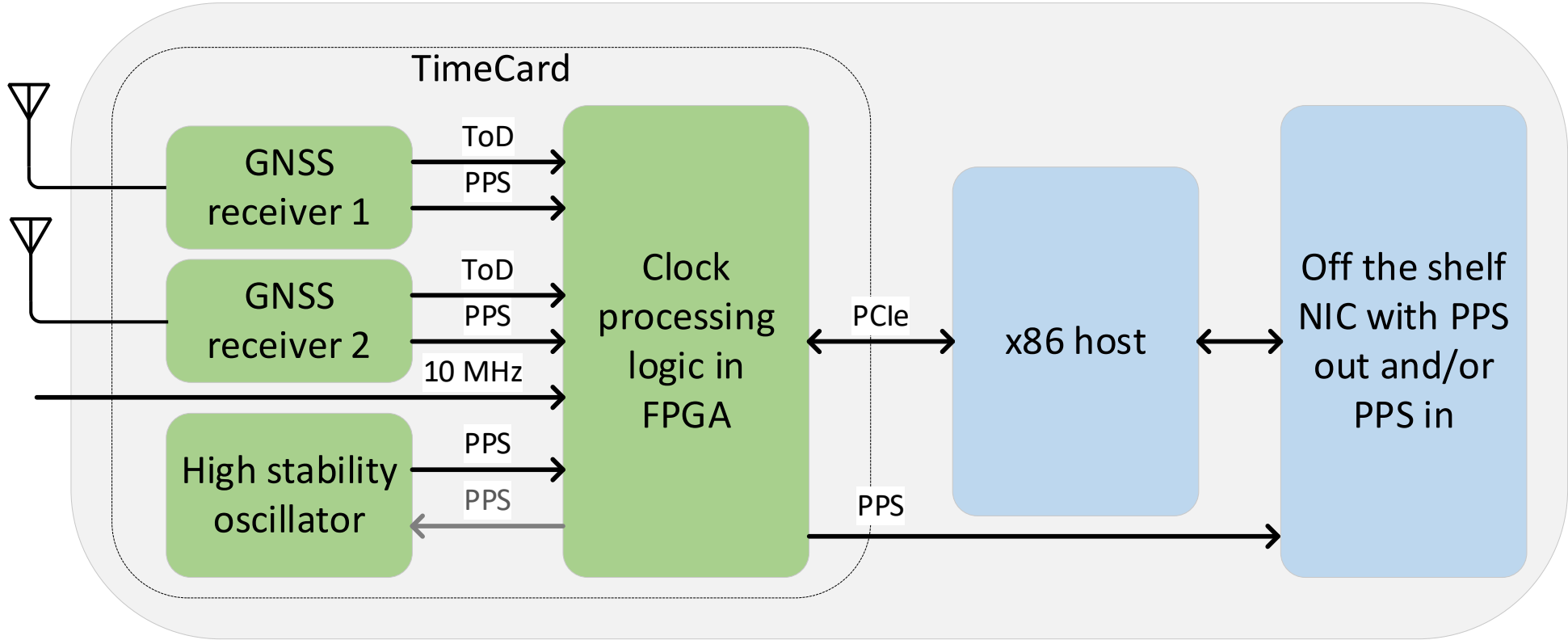


Concept of Time Card





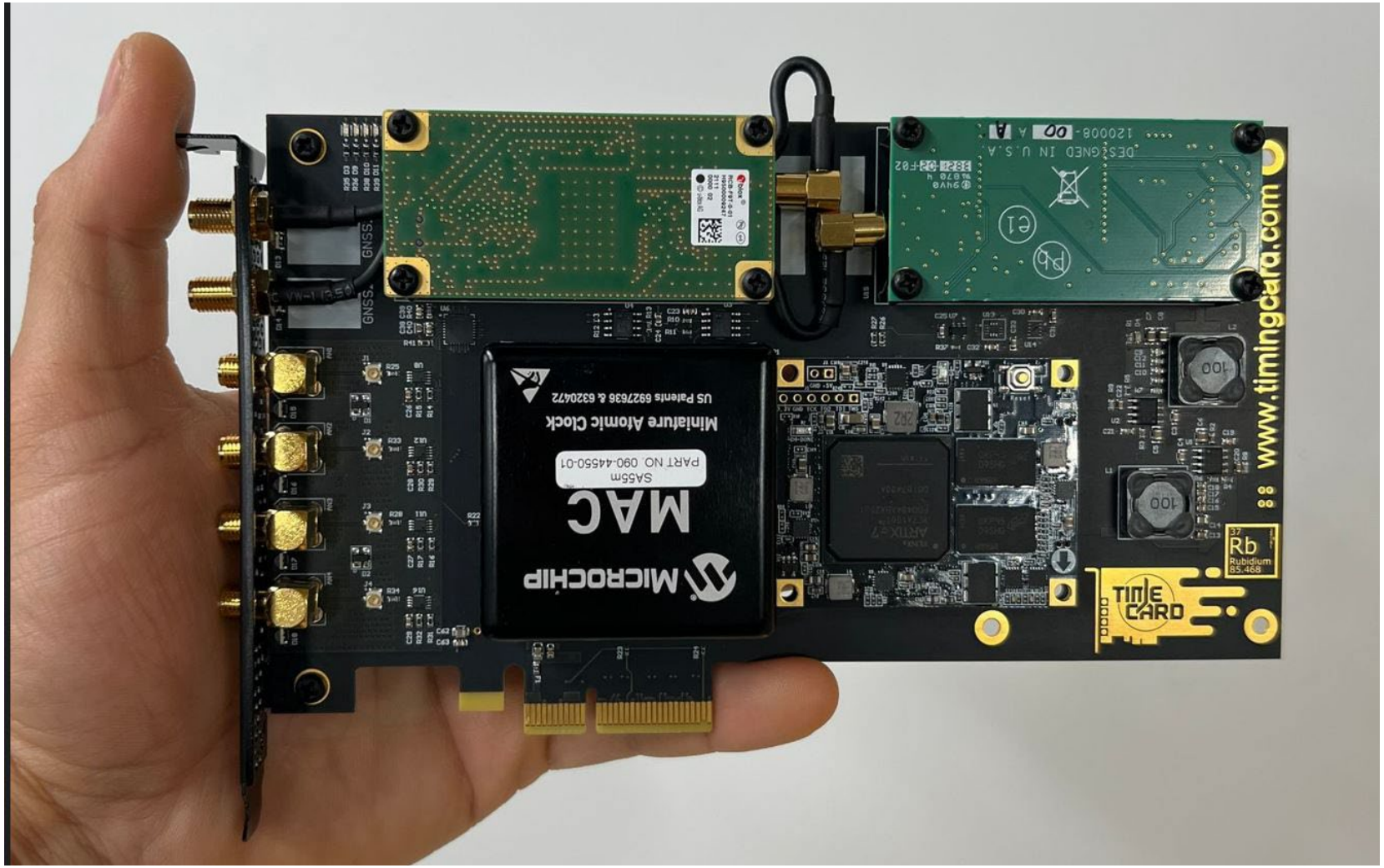
Time Card 2


TimeCard
GNSS receiver 1
GNSS receiver 2
High stability oscillator
ToD
PPS
ToD
PPS
10 MHz
PPS
PPS
Clock processing logic in FPGA
PCIe
x86 host
PPS
Off the shelf NIC with PPS out and/or PPS in

Time Card 2

Highlights:

- Dual GNSS
- PTM Support
- MSI-X
- New Placement
- IRIG-B, DCF77
- more GNSS support
- Freq Gen and Count



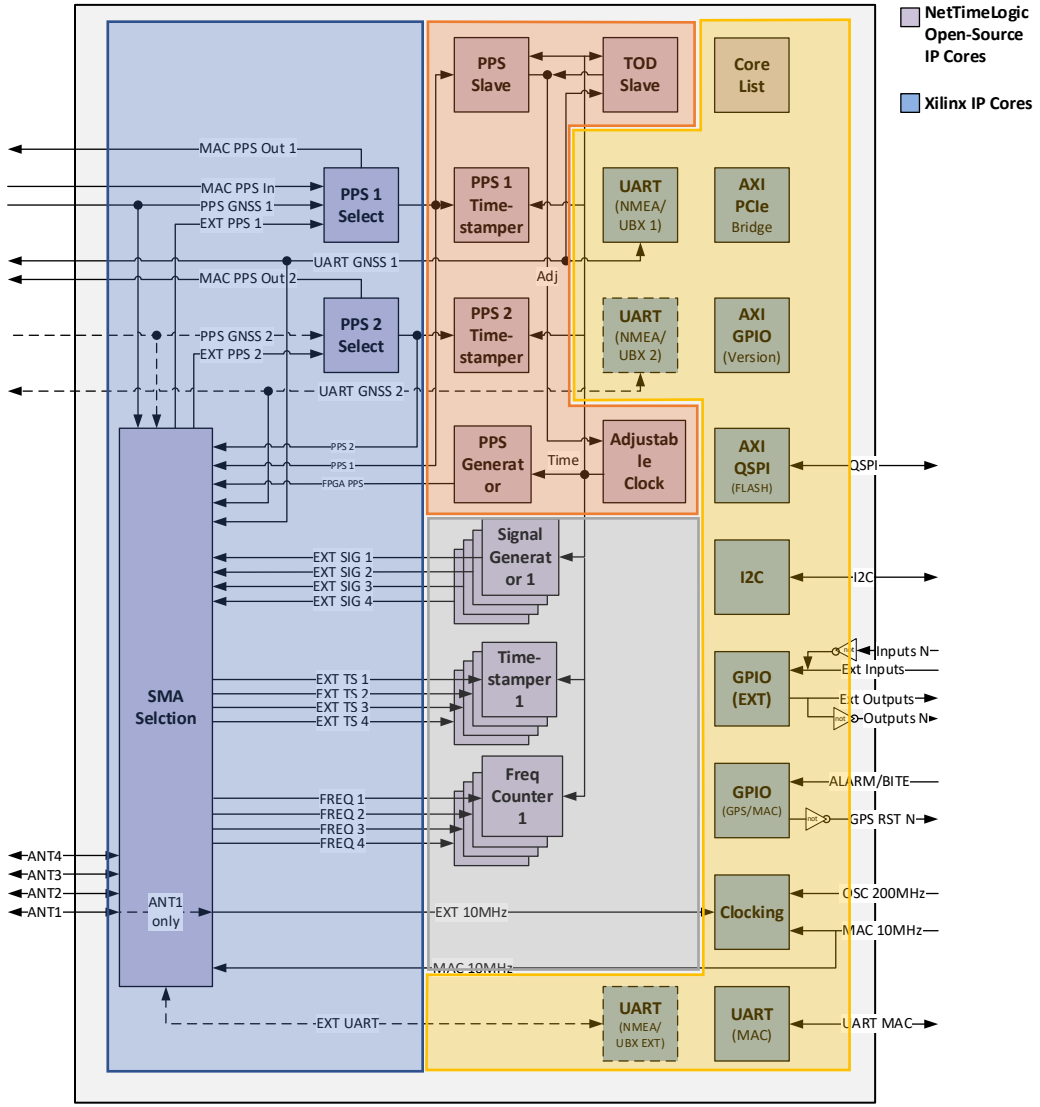
Other Improvements

Support for CSAC

Larger FPGA (XC7200)

SDR based GNSS

Clock Engine Block Diagram



TIME SOURCE SELECTION
Select the time synchronization sources

TIME SYNCHRONIZATION
Standalone FPGA cores of time synchronization

TIME FUNCTIONS
Time-related support functions

CONTROL & COMMUNICATION
Interfaces to CPU and peripherals

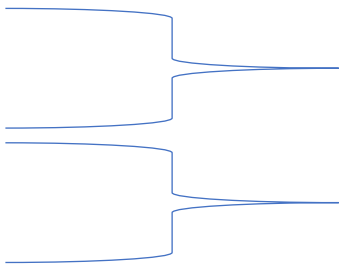
PCIe Memory Map

AXI Slave interface	Slave	Offset Address	High Address
S_AXI_CTL	AXI PCIe Control	0x0001_0000	0x0001_0FFF
axi4l_slave	Version	0x0002_0000	0x0002_0FFF
S_AXI	AXI GPIO Ext	0x0010_0000	0x0010_0FFF
S_AXI	AXI GPIO GPS/MAC	0x0011_0000	0x0011_0FFF
S_AXI	AXI GPIO SEL	0x0013_0000	0x0013_0FFF
S_AXI	AXI GPIO SMA MAP1	0x0014_0000	0x0014_0FFF
S_AXI	AXI GPIO SMA STATUS	0x0014_2000	0x0014_2FFF
S_AXI	AXI I2C	0x0015_0000	0x0015_FFFF
S_AXI	AXI UART 16550 GPS	0x0016_0000	0x0016_FFFF
S_AXI	AXI UART 16550 GPS2	0x0017_0000	0x0017_FFFF
S_AXI	AXI UART 16550 MAC	0x0018_0000	0x0018_FFFF
S_AXI	AXI UART 16550 NMEA	0x0019_0000	0x0019_FFFF
S_AXI	AXI GPIO SMA MAP2	0x0022_0000	0x0022_0FFF
S_AXI_LITE	AXI HWICAP	0x0030_0000	0x0030_FFFF
AXI_LITE	AXI Quad SPI Flash	0x0031_0000	0x0031_FFFF
axi4l_slave	NTL Adj. Clock	0x0100_0000	0x0100_FFFF
axi4l_slave	NTL Signal TS0 (GNSS)	0x0101_0000	0x0101_FFFF
axi4l_slave	NTL Signal TS1	0x0102_0000	0x0102_FFFF
axi4l_slave	NTL PPS Master	0x0103_0000	0x0103_FFFF

AXI Slave interface	Slave	Offset Address	High Address
axi4l_slave	NTL PPS Slave	0x0104_0000	0x0104_FFFF
axi4l_slave	NTL TOD Slave	0x0105_0000	0x0105_FFFF
axi4l_slave	NTL Signal TS2	0x0106_0000	0x0106_FFFF
axi4l_slave	NTL IRIG Slave	0x0107_0000	0x0107_FFFF
axi4l_slave	NTL IRIG Master	0x0108_0000	0x0108_FFFF
axi4l_slave	NTL DCF Slave	0x0109_0000	0x0109_FFFF
axi4l_slave	NTL DCF Master	0x010A_0000	0x010A_FFFF
axi4l_slave	NTL TOD Master	0x010B_0000	0x010B_FFFF
axi4l_slave	NTL Signal TS PPS	0x010C_0000	0x010C_FFFF
axi4l_slave	NTL Signal Generator1	0x010D_0000	0x010D_FFFF
axi4l_slave	NTL Signal Generator2	0x010E_0000	0x010E_FFFF
axi4l_slave	NTL Signal Generator3	0x010F_0000	0x010F_FFFF
axi4l_slave	NTL Signal Generator4	0x0110_0000	0x0110_FFFF
axi4l_slave	NTL Signal TS3	0x0111_0000	0x0111_FFFF
axi4l_slave	NTL Signal TS4	0x0112_0000	0x0112_FFFF
axi4l_slave	Frequency Counter 1	0x0120_0000	0x0120_FFFF
axi4l_slave	Frequency Counter 2	0x0121_0000	0x0121_FFFF
axi4l_slave	Frequency Counter 3	0x0122_0000	0x0122_FFFF
axi4l_slave	Frequency Counter 4	0x0123_0000	0x0123_FFFF

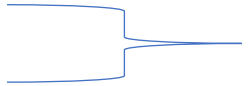
Driver

```
/sys/class/timecard/ocp0 # ls -l
total 0
-r--r--r-- 1 root root 4096 Mar 15 08:56 available_clock_sources
-r--r--r-- 1 root root 4096 Mar 15 08:56 available_sma_inputs
-r--r--r-- 1 root root 4096 Mar 15 08:56 available_sma_outputs
-rw-r--r-- 1 root root 4096 Mar 15 08:56 clock_source
-r--r--r-- 1 root root 4096 Mar 15 08:56 clock_status_drift
-r--r--r-- 1 root root 4096 Mar 15 08:56 clock_status_offset
-rw-r--r-- 1 root root 4096 Mar 15 08:56 config
lrwxrwxrwx 1 root root    0 Mar 15 08:56 device -> ../../../0000:65:00.0
-rw-r--r-- 1 root root 4096 Mar 15 08:56 external_pps_cable_delay
drwxr-xr-x 2 root root    0 Mar 15 08:56 freq1
drwxr-xr-x 2 root root    0 Mar 15 08:56 freq2
drwxr-xr-x 2 root root    0 Mar 15 08:56 freq3
drwxr-xr-x 2 root root    0 Mar 15 08:56 freq4
drwxr-xr-x 2 root root    0 Mar 15 08:56 gen1
drwxr-xr-x 2 root root    0 Mar 15 08:56 gen2
drwxr-xr-x 2 root root    0 Mar 15 08:56 gen3
drwxr-xr-x 2 root root    0 Mar 15 08:56 gen4
-r--r--r-- 1 root root 4096 Mar 15 08:56 gnss_sync
-rw-r--r-- 1 root root 4096 Mar 15 08:56 holdover
lrwxrwxrwx 1 root root    0 Mar 15 08:56 i2c -> ../../xiic-i2c.103424/i2c-10
-rw-r--r-- 1 root root 4096 Mar 15 08:56 internal_pps_cable_delay
-rw-r--r-- 1 root root 4096 Mar 15 08:56 irig_b_mode
-rw-r--r-- 1 root root 4096 Mar 15 08:56 mac_i2c
drwxr-xr-x 2 root root    0 Mar 15 08:56 power
lrwxrwxrwx 1 root root    0 Mar 15 08:56 pps -> ../../../../../virtual/pps/pps3
lrwxrwxrwx 1 root root    0 Mar 15 08:56 ptp -> ../../ptp/ptp15
-r--r--r-- 1 root root 4096 Mar 15 08:56 serialnum
-rw-r--r-- 1 root root 4096 Mar 15 08:56 sma1
-rw-r--r-- 1 root root 4096 Mar 15 08:56 sma2
-rw-r--r-- 1 root root 4096 Mar 15 08:56 sma3
-rw-r--r-- 1 root root 4096 Mar 15 08:56 sma4
lrwxrwxrwx 1 root root    0 Mar  6 17:06 subsystem -> ../../../../../../class/timecard
-rw-r--r-- 1 root root 4096 Mar 15 08:56 tod_correction
-rw-r--r-- 1 root root 4096 Mar 15 08:56 ts_window_adjust
lrwxrwxrwx 1 root root    0 Mar 15 08:56 ttyGNSS -> ../../tty/ttyS4
lrwxrwxrwx 1 root root    0 Mar 15 08:56 ttyGNSS2 -> ../../tty/ttyS5
lrwxrwxrwx 1 root root    0 Mar 15 08:56 ttyMAC -> ../../tty/ttyS6
lrwxrwxrwx 1 root root    0 Mar 15 08:56 ttyNMEA -> ../../tty/ttyS7
-rw-r--r-- 1 root root 4096 Mar  6 17:06 uevent
-rw-r--r-- 1 root root 4096 Mar 15 08:56 utc_tai_offset
```

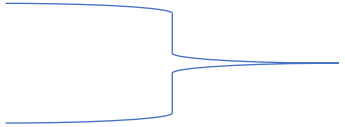


Frequency Counter

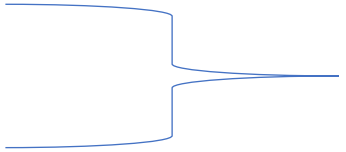
Frequency Generator



PHC (POSIX Clock)



SMA Connectors



Serial Ports

Open Source: timingcard.com

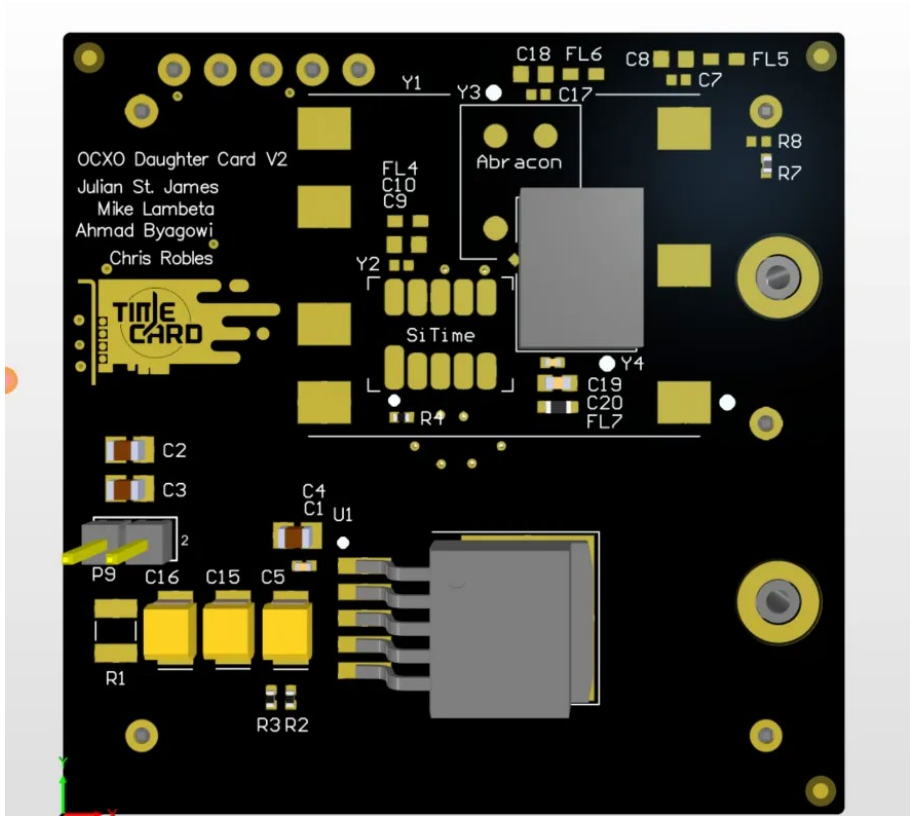
master ▾ Time-Appliance-Project / Time-Card /

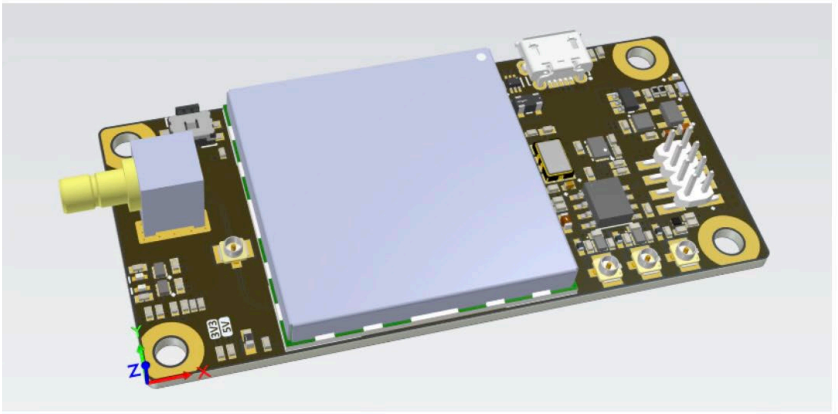
julianstj1 Uploading Celestica Production files	
..	
DOC/Artwork	add new stickers
DRV	Update ptp_ocp.c
FPGA	Added new video to the FPGA tutorial list
GNSS	Add files via upload
HW	Uploading Celestica Production files
OSC	SA45 Daughter Card Commit
SOM	Corrected wording of AXI GPIO SMA STATUS
TEST	Update SSD1327.sh
images	Time Drive V2 WIP

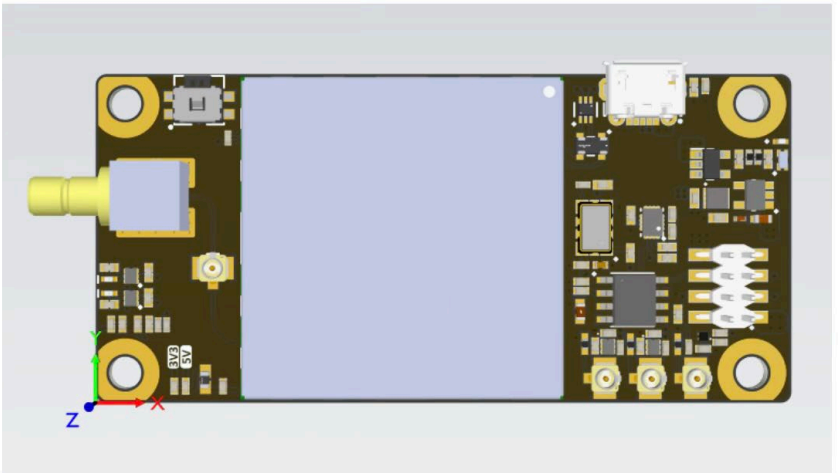
IEEE P3335

- Standard for Architecture and Interfaces for Time Card
- Interoperability
- Community Support
- Wider adoption
- more feedback

RCB and LOF modules

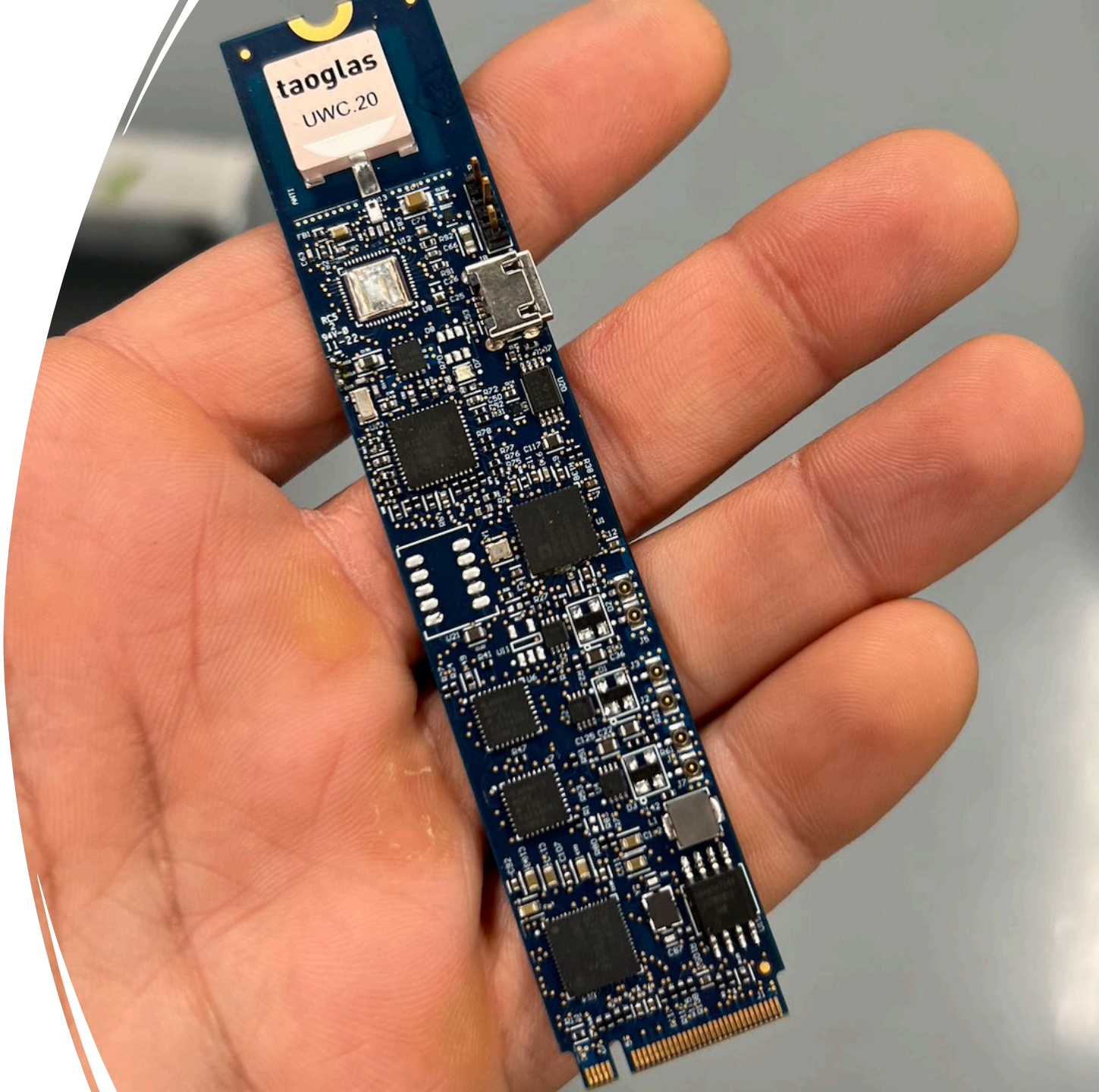






What is Coming Next

- Miniaturization



Thank you

- Join us on:
  - OpenTimeServer.com
  - TimeCard.ch
  - Timingcard.com
  - OCPTAP.com
  - Discord Server : https://discord.gg/rQUKJsHs