Complexity of accurate timestamping on Ethernet

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Timestamping in 1588

- Per IEEE Std 1588-2019 timestamps are supposed to be aligned to the reference plane
  - the reference plane is "*the boundary between PTP Instance hardware and the PTP Network medium*"
  - the 1588 "reference plane" maps to the 802.3 "MDI" (Media Dependent Interface, effectively the connector where the Ethernet fiber/cable/wire in plugged-in)
- IEEE Std 1588-2019 allows the timestamp to be captured at a different point than the reference plane and recommends that the time be corrected for the latency
- IEEE Std 1588-2019 Figure 26 (shown to the right) shows the relationship between these different points

IEEE Std 1588-2019
IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems

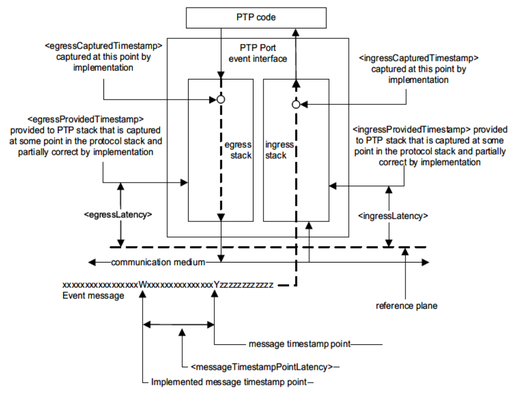
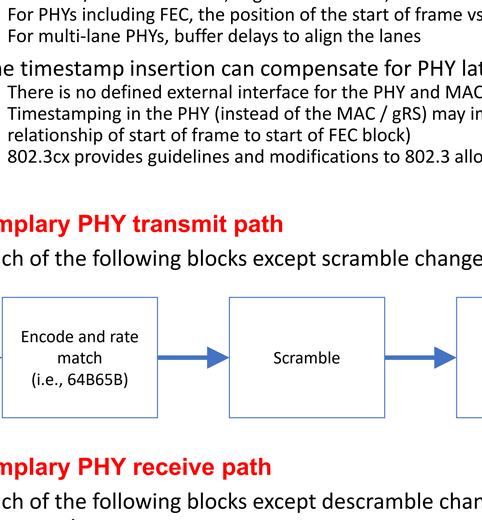


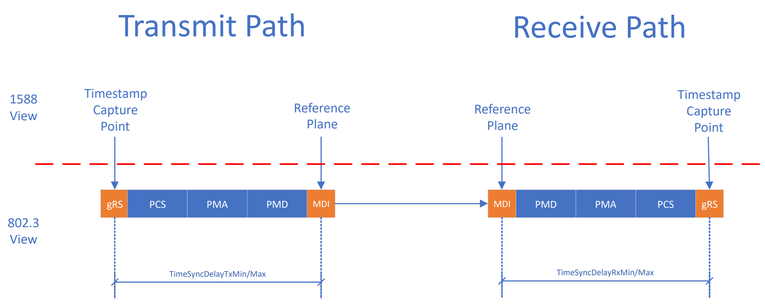
Figure 26—Definition of latency constants



802.3 Delay Measurement Points

- Per 802.3, timestamps are measured at the generic Reconciliation Layer (gRS)
- 1588 uses timestamps representing the Media Dependent Interface (MDI)
- Between the two is the PHY plus Media Dependent Interface (MII)
- 802.3-2018 uses the estimated "data delay" (provided as a min and max value) to compensate for the PHY delay in the timestamps
  - IEEE p802.3cx corrects "data delay" to "path data delay"
- Per 802.3-2018, timestamps are measured at of start of SFD (this conflicts with 1588 which recommends symbol after SFD)

Relationship of 1588 terms to 802.3 terms

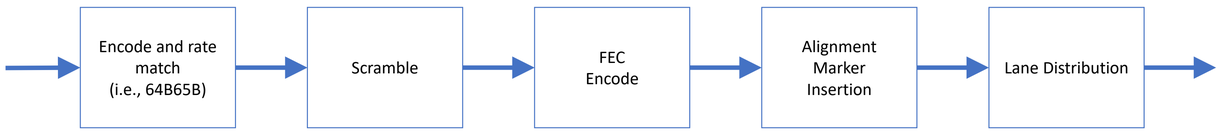


PHY latency variation

- PHY latency relates to the delay from MDI to MII in the Rx direction and from MII to MDI in the Tx direction
- PHY latencies vary due to multiple factors including
  - Different clock rates used
  - Buffers of varying length
  - Clock domain crossings
  - Insertion / removal of idles, alignment markers, and codeword markers
  - For PHYs including FEC, the position of the start of frame vs. the FEC block start
  - For multi-lane PHYs, buffer delays to align the lanes
- The timestamp insertion can compensate for PHY latency if the PHY latency is known
  - There is no defined external interface for the PHY and MAC to share this latency information
  - Timestamping in the PHY (instead of the MAC / gRS) may improve this as the PHY can compensate for its internal state (i.e. relationship of start of frame to start of FEC block)
  - 802.3cx provides guidelines and modifications to 802.3 allowing this to be done

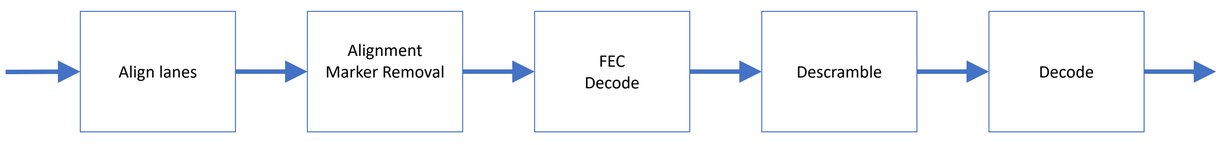
Exemplary PHY transmit path

- Each of the following blocks except scramble changes data rates and Introduces potential timestamp inaccuracies



Exemplary PHY receive path

- Each of the following blocks except descramble changes data rates and Introduces potential timestamp inaccuracies



Proposed 802.3cx Ethernet timestamping improvements

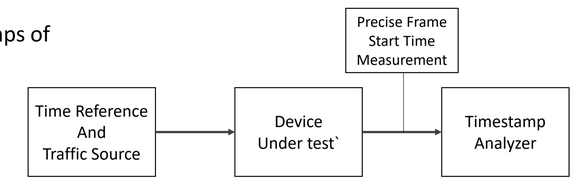
- 802.3cx aims to improve 802.3 timestamping, aligning with the 1588 requirements, removing ambiguity, and increasing both precision and accuracy
- Supports bit-level timestamps at the xMII interface (rather than timestamping the entire xMII word)
- Provides a mechanism in the 802.3 spec for a PHY to report the dynamic PHY delay changes to the MAC
- Enables configuration of either the first symbol of frame data or first symbol of SFD as the delay measurement point in the frame
- Clarifies timestamps behavior on multi-lane PHYs
- Maintains timestamp accuracy with insertion/removal of IDLE
- Specifies recommendations for handling different symbol sizes at the MDI (see below)
- Adds support for sub-ns (units of 2^{-16} ns) timestamping resolution

Limits of 802.3cx

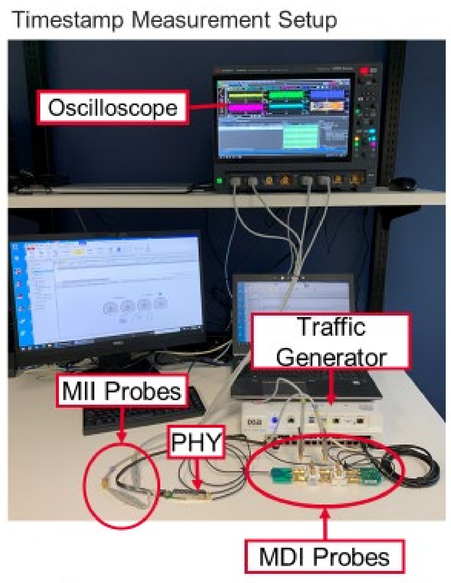
- To maintain backwards compatibility, most of 802.3cx changes are only recommendations (normative "should" statements or, more often, just informative text)
  - Multiple such recommendations are in an informative annex (annex 90A)
- Except for delay measurement point (SFD or first symbol after SFD), there is no management interface determining which of the options are used for a given implementation
- Without internal knowledge, a 1588 or 802.1AS implementation cannot compensate

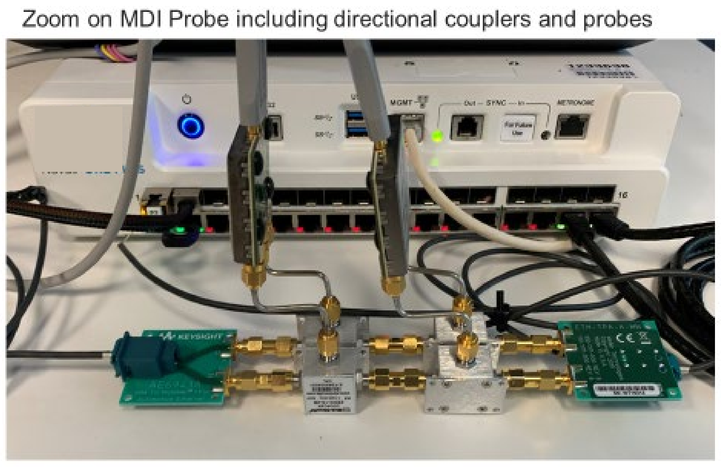
Latency and timestamping characterization

- Connect test equipment to the DUT such that the time the frame starts can be ascertained at MDI interface
  - Both Tx and Rx direction measurements are needed
- Send traffic through the DUT and measure the timestamps of hundreds of thousands of frames
- Must test a mix of different frame types & sizes
  - Must test with different inter-frame gaps, including minimum
  - Instrumentation must support measuring delay of consecutive frames
  - Instrumentation must validate that received frame matches transmit frame (any corrupted frames need to be excluded; guarantees that we are comparing the same frame at input and output)



Sample timestamp accuracy measurement setup

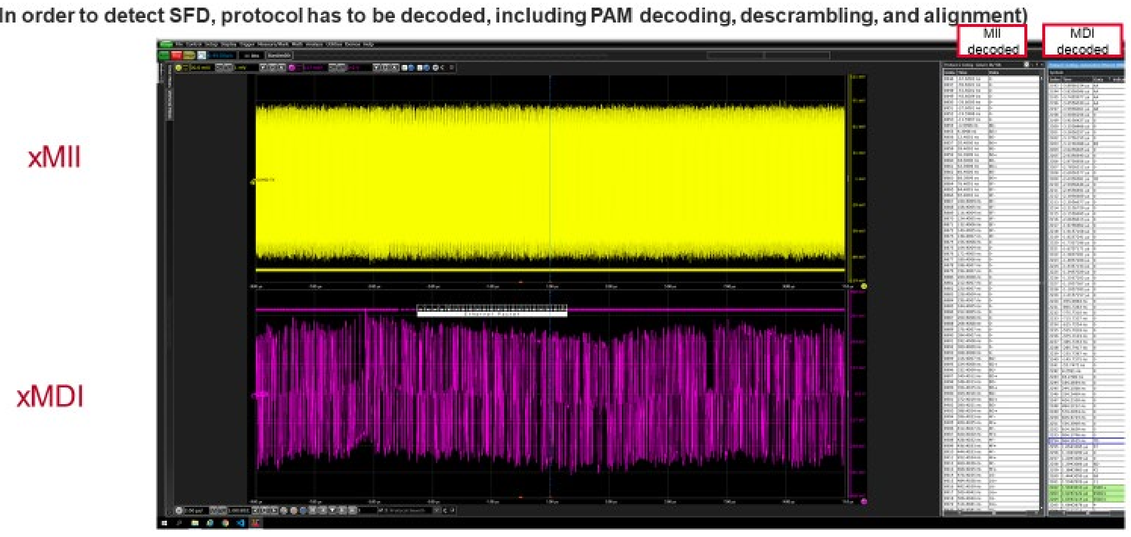




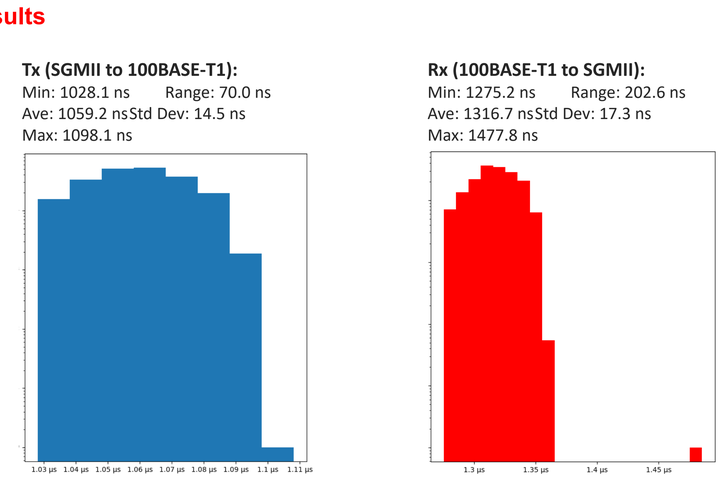
MII = Media Independent Interface (defined in IEEE Std. 802.3)
MDI = Media Dependent Interface (defined in IEEE Std. 802.3)
DUT = Device Under test

Protocol decode

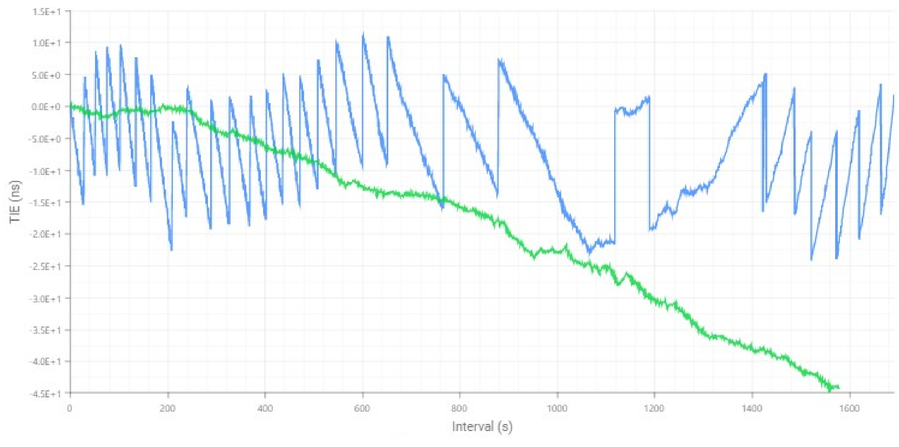
In order to detect SFD, protocol has to be decoded, including PAM decoding, descrambling, and alignment)



Sample Results



PHY timestamp variation on 100BASE-T1 PHY



PHY timestamp variation in 10GBASE-X causing poor sync performance in local servo