Module latency and impact on timing performance

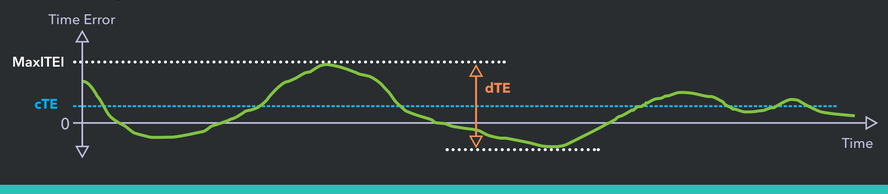
Calnex
Insight and Innovation

What are the issues?

- As the end-to-end timing requirements of systems become lower, the time error impact of inserted optical modules becomes an increasingly significant factor.
- Contributing factors to Time Error are latency variations in service (dTE), run-to-run latency variations and asymmetric latency (cTE)

T-BC / T-TSC / T-TC	cTE	dTE (MTIE)	maxITEI	dTE (high-pass filtered)
Class A (with SyncE)	±50 ns	40 ns	100 ns	70 ns
Class B (with SyncE)	±20 ns	40 ns	70 ns	70 ns
Class C (with eSyncE)	±10 ns	10 ns	30 ns (T-BC) Under Study for T-TC	Under Study
Class D (with eSyncE) (Only T-BC and T-TSC)	Under Study	Under Study	5 ns	Under Study

Constant and Dynamic Time Error (cTE and dTE)



What are the issues?

From MOPA (Mobile Optical Pluggables Alliance) technical paper:

"System vendors, pluggable vendors and DSP vendors can collaboratively make future DSP-based optics more "timing and sync friendly" by characterizing and putting a cap on the propagation delay asymmetry so that the overall contribution of optical pluggables can be engineered in the complete system."

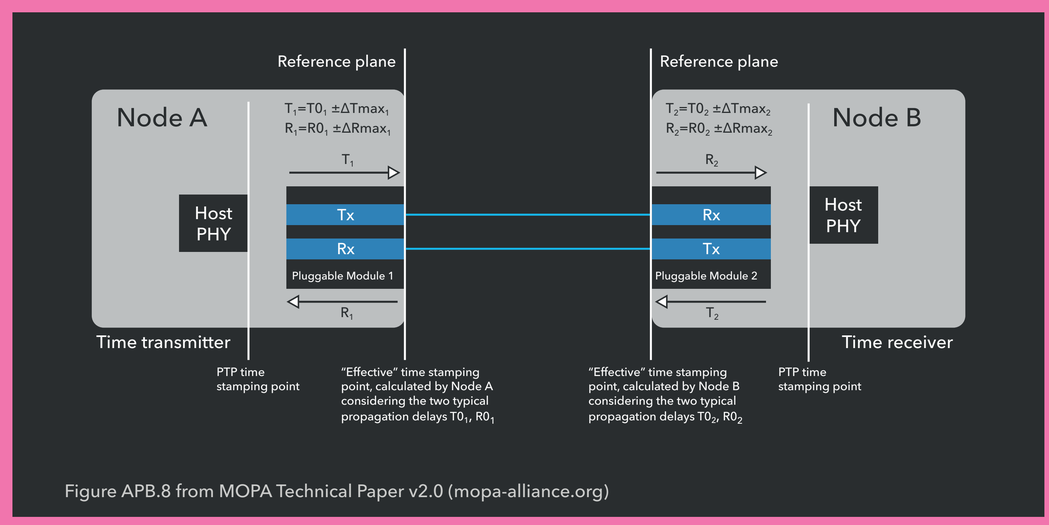


Figure APB.8 from MOPA Technical Paper v2.0 (mopa-alliance.org)

Specifying module performance and uncertainty

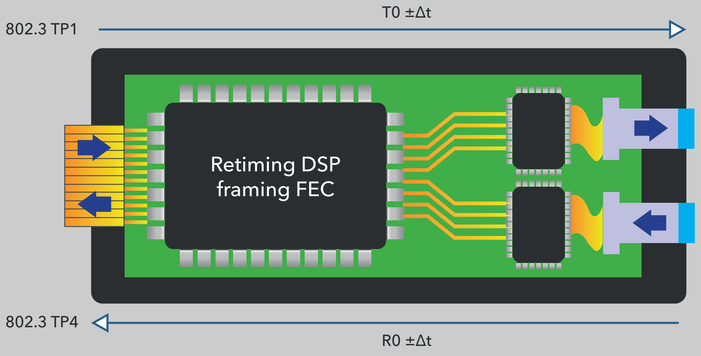
MOPA proposes to specify Classes of Optical Modules, based on the Class of Network Device they are intended to work with, and the percentage of the Time Error budget that should be allocated to the module.

Example of module maximum error for use with ITU-T G.8273.2 Class B nodes:

	Class B.10	Class B.20
Max constant time error budget allocated to one pluggable	±2 ns	±4 ns

This will be supported with a 'Guaranteed by Design' approach, so that individual modules are not required to be tested in production.

Similar to the approach for timing systems themselves, a statistically significant percentage of modules would be measured during Design Validation Test.



Confidence via direct test

A possible approach to verify the performance of optical modules (i.e. asymmetry between Rx and Tx) has been presented at last ITSF. This consists of a two-step approach.

1. Measure total latency through a pair of optical modules with a loop back connection and using systems with performance timestamping (see Figure 1).
2. Isolating Tx latency as shown in Figure 2; the Rx latency can hence be derived from measurements of Toltal Latency and Tx Latency.

Figure 1. Example loopback set up to test total latency across a pair of PAM4 modules

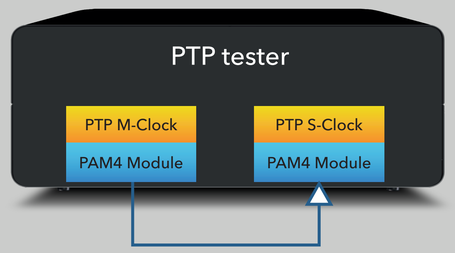
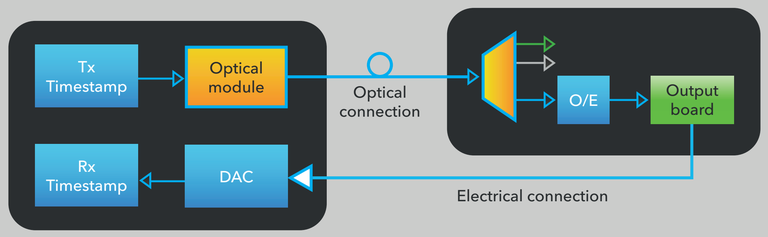


Figure 2. Example measurement set up to estimate the Tx latency



Potential 'step-by-step' process for measurement and validation

Step 1
Characterise delay through O/E using low-latency 25G NRZ optics.

Step 2 – PTP based measurement
Perform precision T1 measurement – Unidirectional measurement. This leverages existing technology for nanosecond level packet timestamping.

Step 3 – Pattern based measurement
Inject "bespoke pattern" at physical layer to measure optics at 28Gbaud and 56Gbaud.