VIRTUAL TUTORIAL

SYNCHRONIZED CLOCKS

FEBRUARY 2023
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OUTLINE

- Time, Phase & Frequency
- Phase Locked Loops (PLL)
  - Principle
  - Response To Injected Noise
  - Operation Modes
- Clock Combining

TIME, PHASE & FREQUENCY

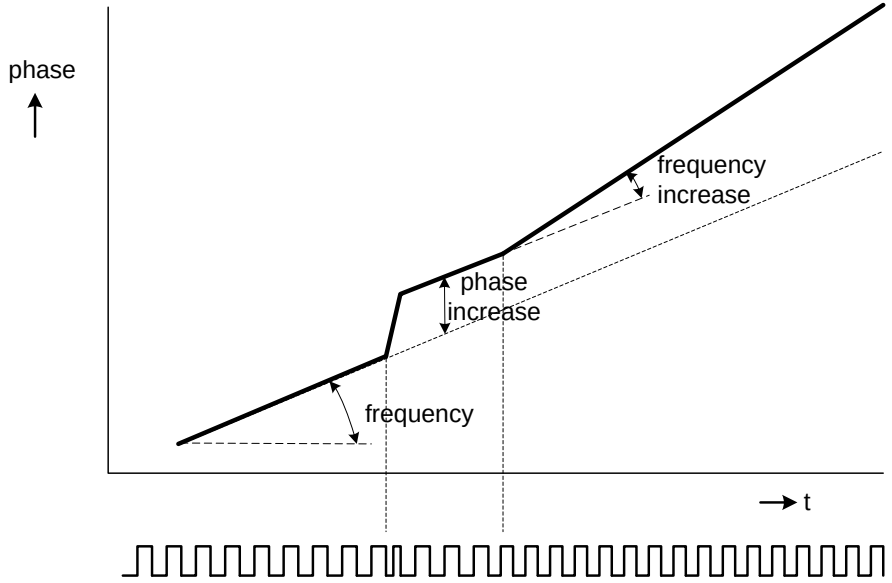
We all know what time is. Unit is second [s]

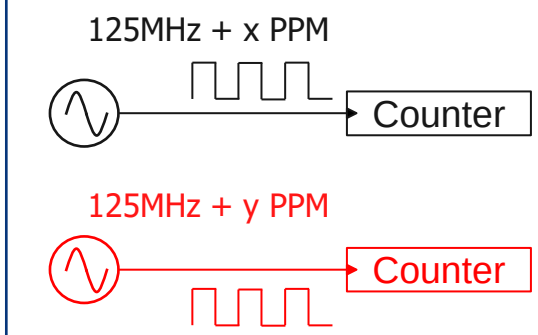
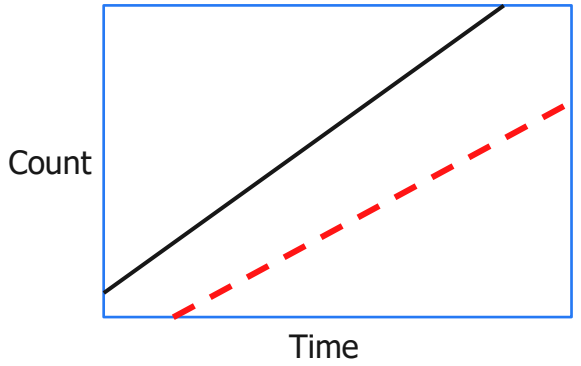
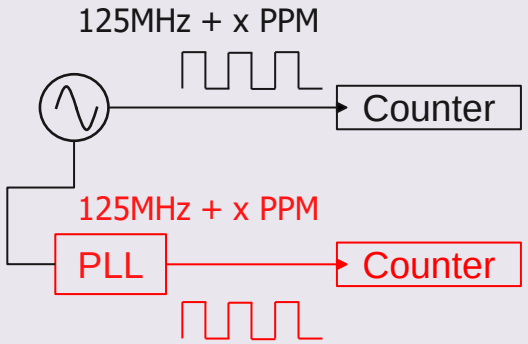
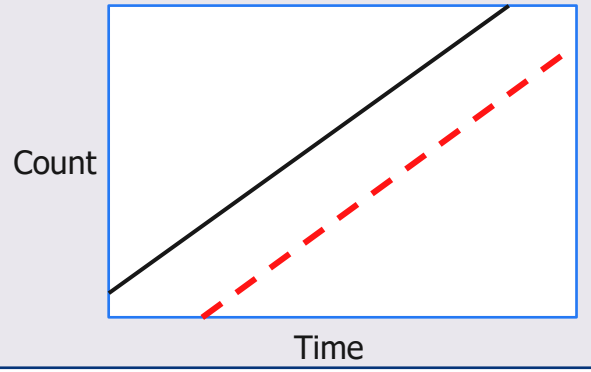
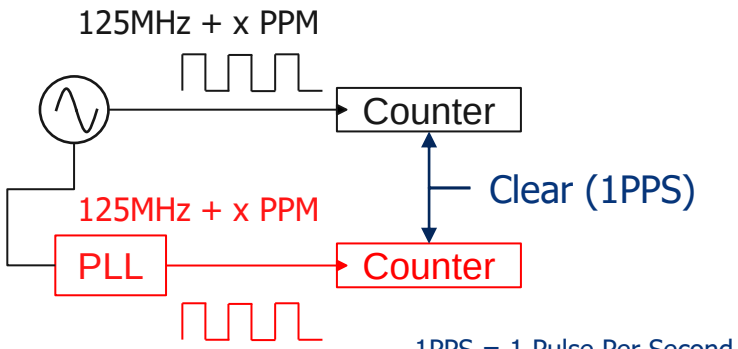
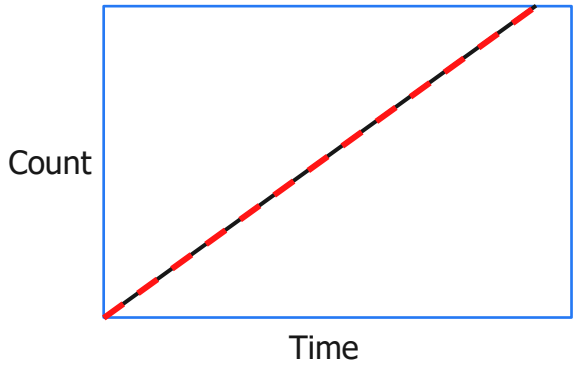
Phase is the angle of a rotating vector.

- In clock terms: phase is time related to the period of a repetitive signal.
- Phase = time/period * 2π, unit is radians [rad]

Frequency is a statistical term; number of events per second. Unit is Hertz [Hz]

Jitter, wander, phase noise is a variation of the clock's frequency/period/phase. It is essentially a phase modulation of the carrier clock.



		Not Synchronized
		Frequency Synchronized (Syntonized)
		Phase/Time Synchronized

PHASE LOCKED LOOPS (PLL)

PRINCIPLE

WHAT DOES A PLL DO?

A phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal

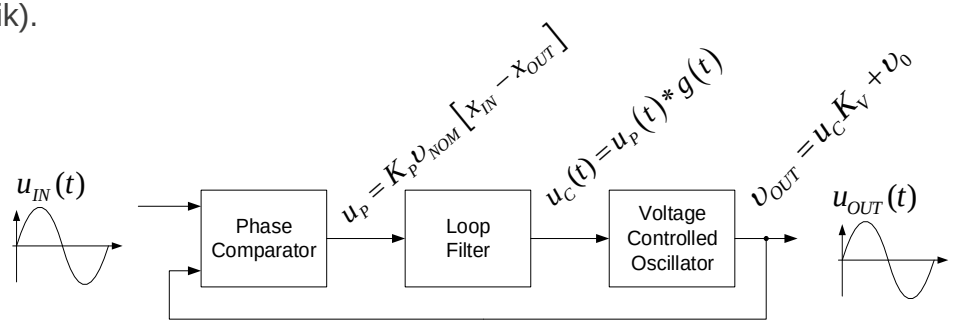
- Bringing the output signal back to the input signal for comparison is called a feedback loop

Generate a clock that is phase and frequency locked to an input clock.

- The output clock frequency can be of the same frequency, an integer multiple or a fraction of the input clock frequency.
- Input edge to output edge phase alignment can be achieved.

Input clock frequency to output clock frequency ratio must be a positive integer or fractional number.

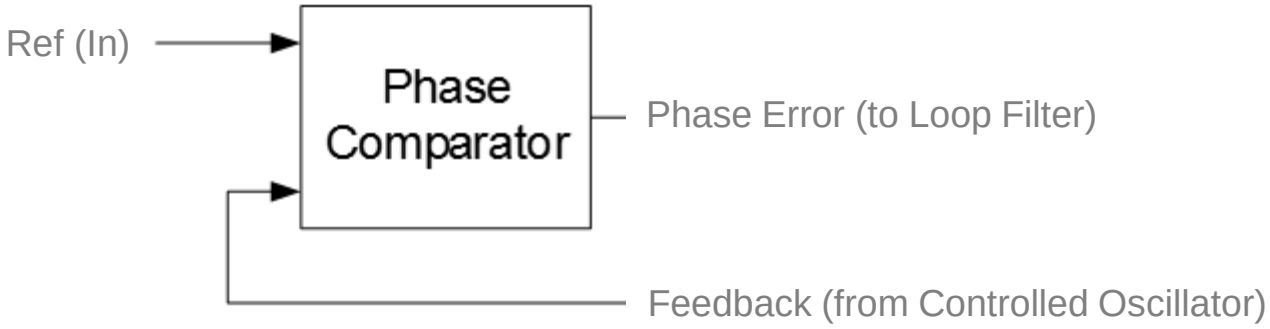
- 19.44 MHz to 66/64*255/237*78125/77760*622.08 MHz is possible.
- 10 MHz to π MHz is not possible (afaik).



$$u_{IN}(t) = A \cdot \sin\left\{2\pi\upsilon_{NOM}\left[t + x_{IN}(t)\right]\right\} = A \cdot \sin\left\{2\pi\upsilon_{IN}(t) + \varphi_{0,IN}\right\}$$

$$u_{OUT}(t) = A \cdot \sin\left\{2\pi\upsilon_{NOM}\left[t + x_{OUT}(t)\right]\right\} = A \cdot \sin\left\{2\pi\upsilon_{OUT}(t) + \varphi_{0,OUT}\right\}$$

PLL BUILDING BLOCKS: PHASE COMPARATOR



The Phase Comparator establishes the “error” between the reference input and the clock output; using a feedback

Most Digital PLLs (DPLLs) use a Time to Digital Converter (TDC) for the Phase Frequency Detector (PFD) to measure the phase of the two clocks and produce a digital word representing the error

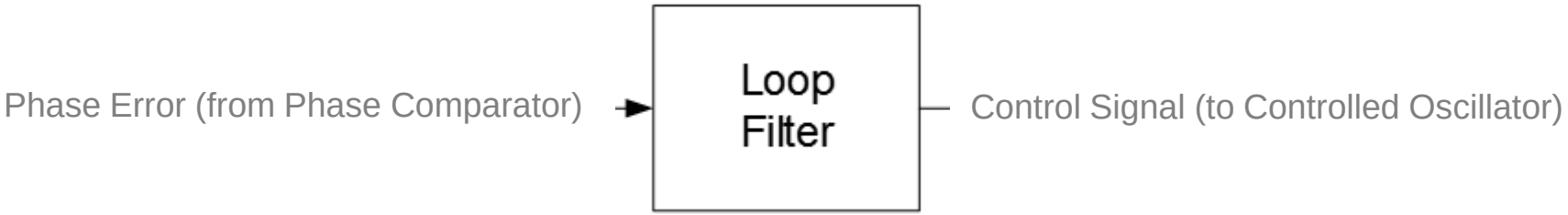
- TDC can be looked at as a timestamper, resolution determined by the sampling clock

The TDC timestamps the reference and feedback edges, and the PFD mathematically tracks the phase offset between the selected reference and feedback clocks

The measured phase difference can go well beyond 1 period, or Unit Interval (UI), of the reference and feedback clocks; thus, the phase comparator must be able to measure over a large range of multiple input/feedback clock periods

- Various telecom standards define a jitter & wander tolerance requirement - the widest is defined is $18\mu s_{p\text{-}p}$
- For example, if the input clock has a nominal period of 8ns (125 MHz), then the jitter tolerance requirement equates to ± 1125 UI

PLL BUILDING BLOCKS: LOOP FILTER



The phase error is processed by the loop filter (LF) or low-pass filter (LPF), which filters out high frequency phase noise (jitter)

- LF is a combination of proportional and integral (PI) control, which generates a control signal for controlling the oscillator
- The integrator is an additional pole, therefore 2nd order (may be referenced as “Type 2” PLL)

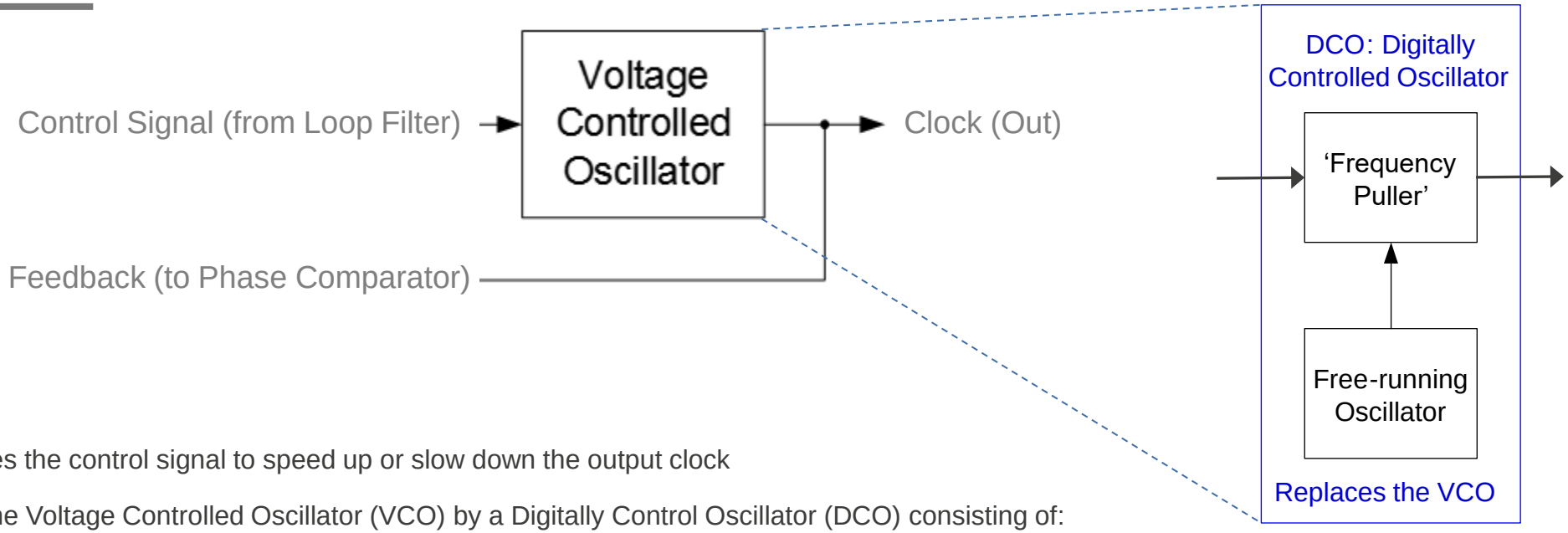
The LF determines the bandwidth (BW) of the PLL (i.e. cut-off frequency)

- Other functionality, such as phase slope limiting (PSL), locking range, and holdover functionality may be done as well

The step response has an overshoot and the frequency domain transfer function has peaking.

- Phase corrections mainly done through proportional path, along with any PSL
- Frequency offset, or drift corrections, is done through the integrator path, including damping (i.e. gain peaking control)

PLL BUILDING BLOCKS: CONTROLLED OSCILLATOR

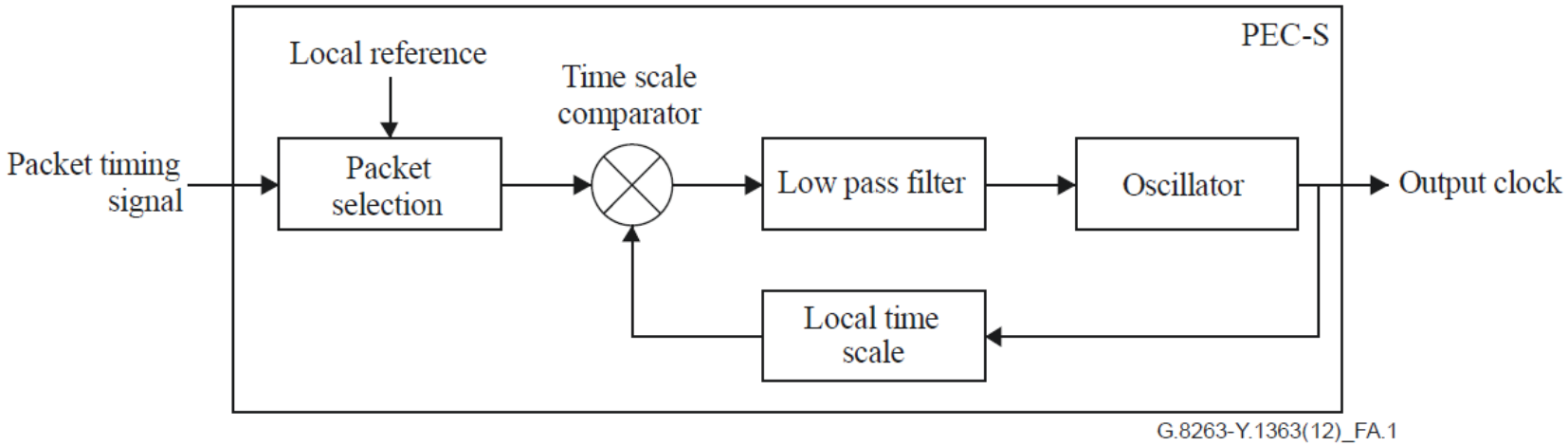


The controlled oscillator uses the control signal to speed up or slow down the output clock

Most Digital PLLs replace the Voltage Controlled Oscillator (VCO) by a Digitally Control Oscillator (DCO) consisting of:

- a free-running crystal oscillator (XO)
- A digital synthesizer which pulls the frequency up or down using a Control Signal from loop filter (a digital word representing a fractional frequency offset (FFO))

PLL: USE WITH PACKET CLOCKS



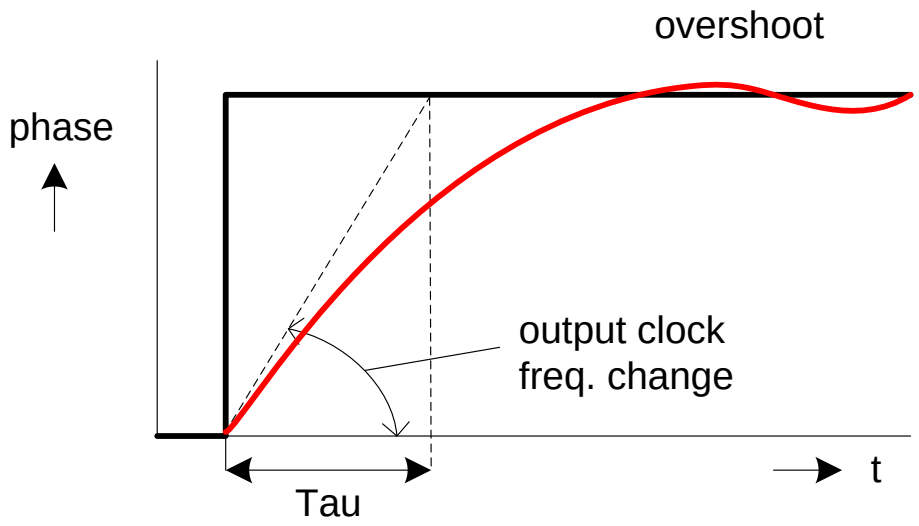
A timing protocol, such as IEEE 1588, can be used as the phase (or time) comparator

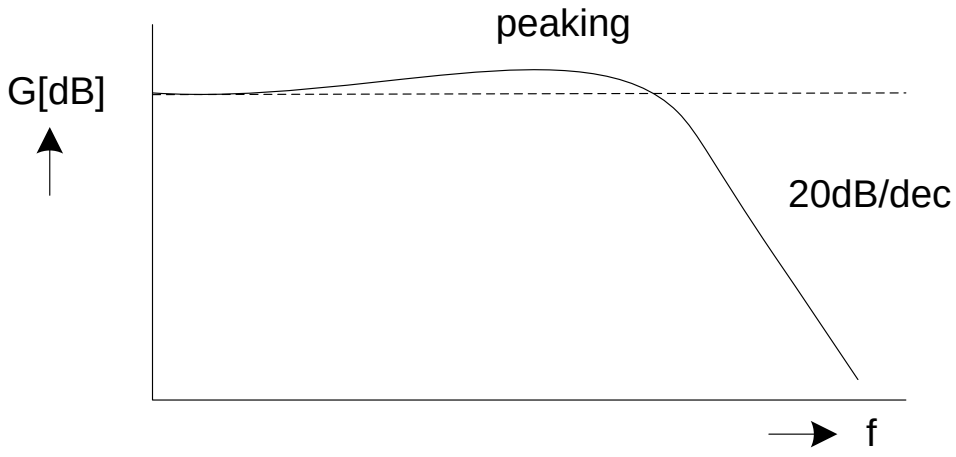
- Still follows same model as PLL, but may introduce a packet selection block
- Without packet selection, the packet delay variation (PDV) will have a significant impact to the loop filter

The LF will typically be designed to support much lower update intervals of the phase error

- This is due to packet dropping, or to attenuate the impact of the PDV
- Typically requires a more stable local clock source (oscillator, or maybe physical layer assistance)

PLL: STEP RESPONSE & JITTER TRANSFER OF A TYPE 2 DPLL





PHASE LOCKED LOOPS (PLL)

RESPONSE TO INJECTED NOISE

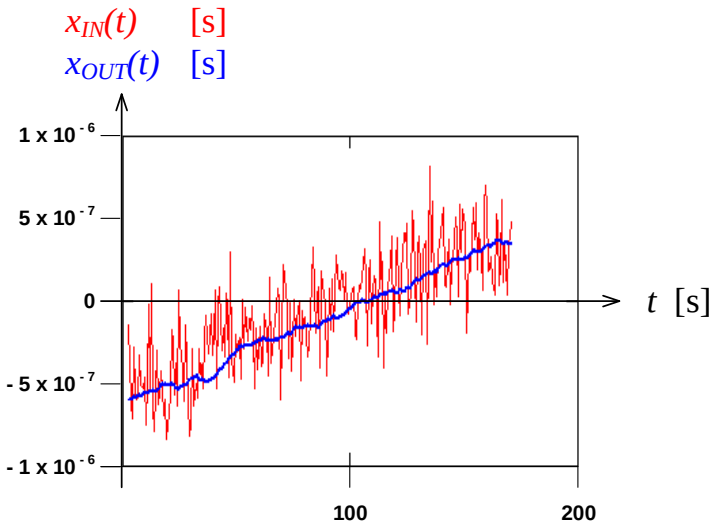
PLL: JITTER & WANDER FILTERING

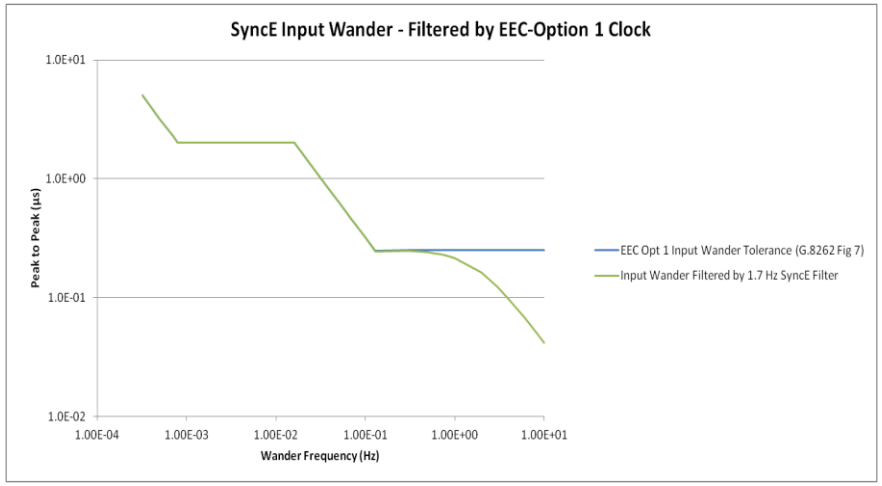
What is jitter/wander?

- Noise or other disturbances on the clock when compared to an ideal reference
  - Jitter = short-term variations
  - Wander = long-term variations
- ITU-T G.810 defines noise frequencies <10Hz as wander and frequencies ≥10Hz as jitter

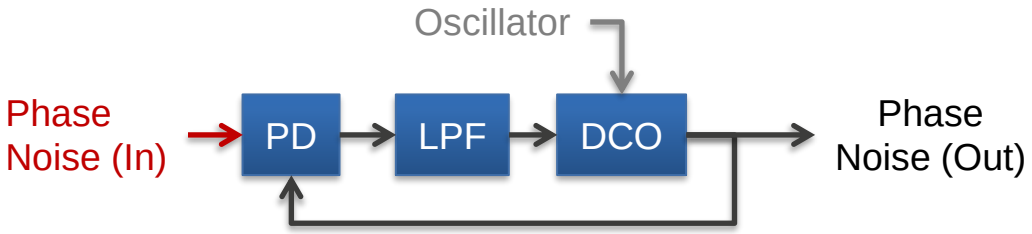
The function of a PLL is to attenuate jitter and transfer wander

- In other words, tolerate noise at the input without losing lock to the reference

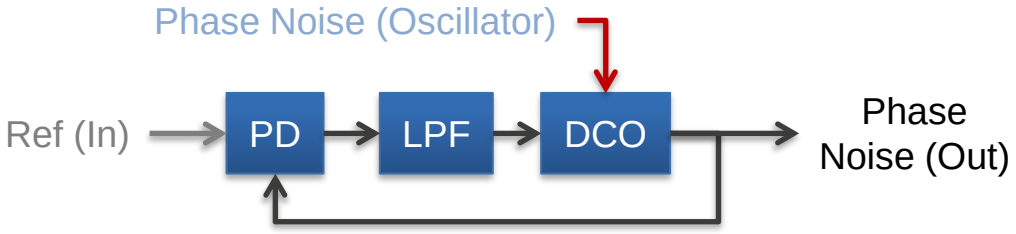




PLL: RESPONSE TO INJECTED NOISE

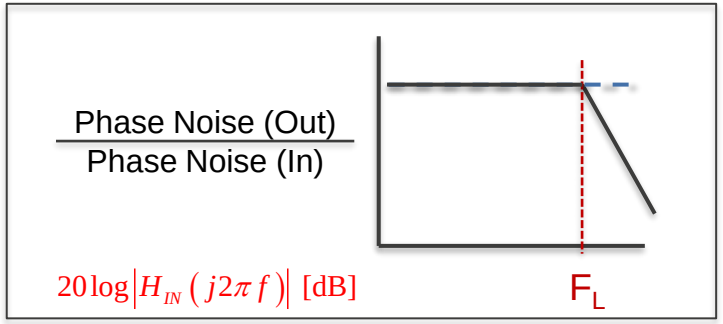


$$x_{OUT}(t) = x_{IN}(t) * h_{IN}(t)$$
$$X_{OUT}(s) = X_{IN}(s) \cdot H_{IN}(s)$$
where $h_{IN}(t) =$ impulse response
$$H_{IN}(s) = \text{transfer function} = \text{Laplace}\{h_{IN}(t)\}$$

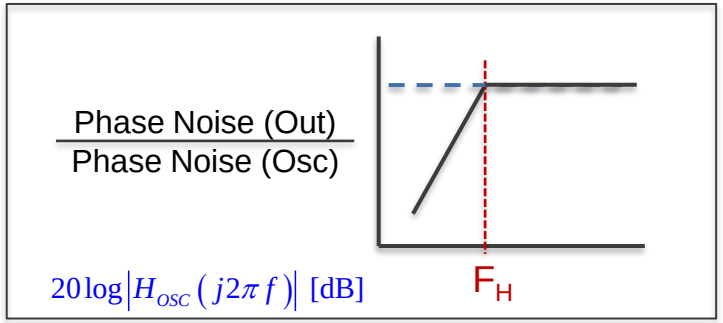


$$x_{OUT}(t) = x_{OSC}(t) * h_{OSC}(t)$$
$$X_{OUT}(s) = X_{OSC}(s) \cdot H_{OSC}(s)$$
where $h_{OSC}(t) =$ impulse response
$$H_{OSC}(s) = \text{transfer function} = \text{Laplace}\{h_{OSC}(t)\}$$

PLL is a low-pass filter for input noise



PLL is a high-pass filter for oscillator noise



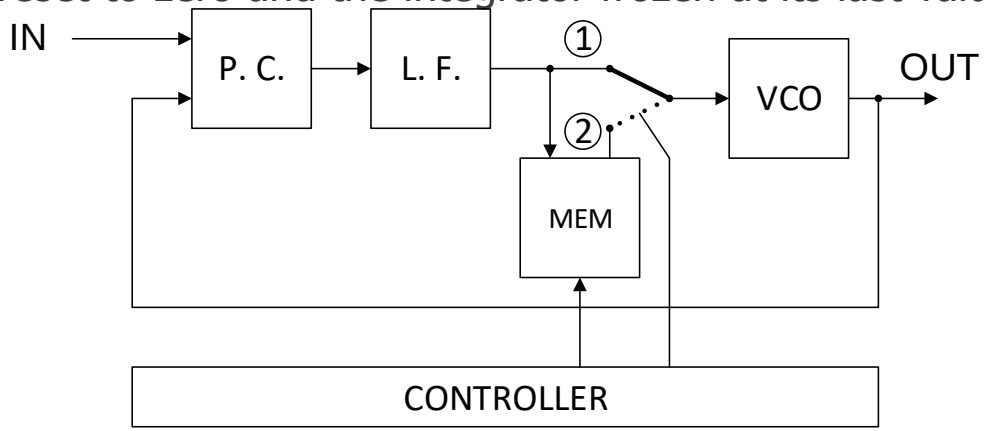
PHASE LOCKED LOOPS (PLL)

OPERATING MODES

PLL MODES: LOCKED, HOLDOVER AND FREERUN

- Freerun mode; the DPLL does not track any input clock. The output clock is at the centre frequency, offset is zero.
- i.e. switch is open.
- Normal / Lock mode; the DPLL tracks the input clock. The output clock is phase & frequency locked to the input clock.
  - i.e. switch is in position 1.
- Holdover mode; Typically used when the input clock fails. The PLL no longer tracks its input clock but uses the last valid frequency offset from memory (MEM). The proportional path is reset to zero and the integrator frozen at its last value. The phase detector is reset to flush out its phase history.
  - i.e. switch is in position 2.
  - clock becomes an autonomous synchronization source

In freerun mode or after entry into holdover mode, frequency is subject to ageing drift and to the influence of temperature.



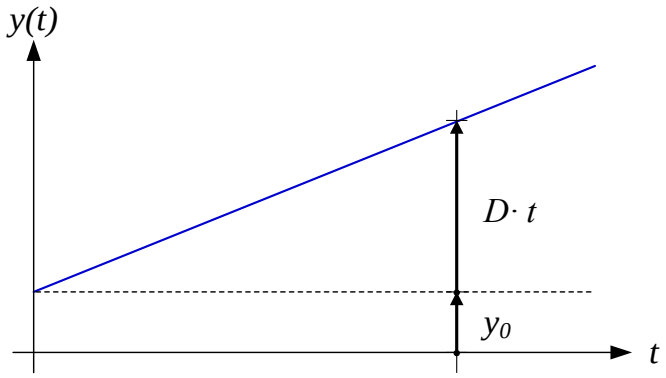
PLL MODES: HOLDOVER @ CONSTANT TEMPERATURE

Fractional frequency:

$y(t) = y_0 + D \cdot t$

where $y_0 =$ initial frequency offset

$D =$ frequency drift rate (constant)



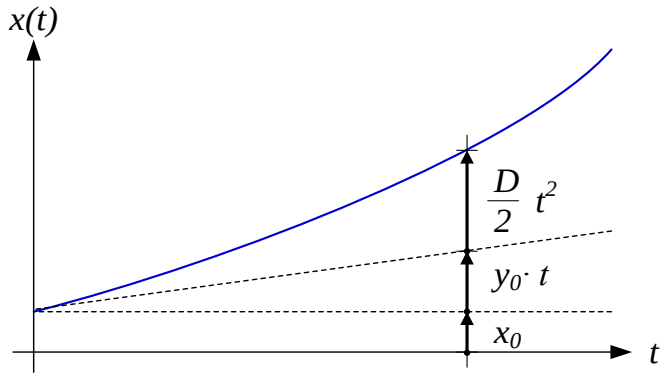
Time error:

$$x(t) = x_0 + y_0 \cdot t + \frac{D}{2} \cdot t^2$$

where $x_0 =$ initial phase offset

$y_0 =$ initial frequency offset

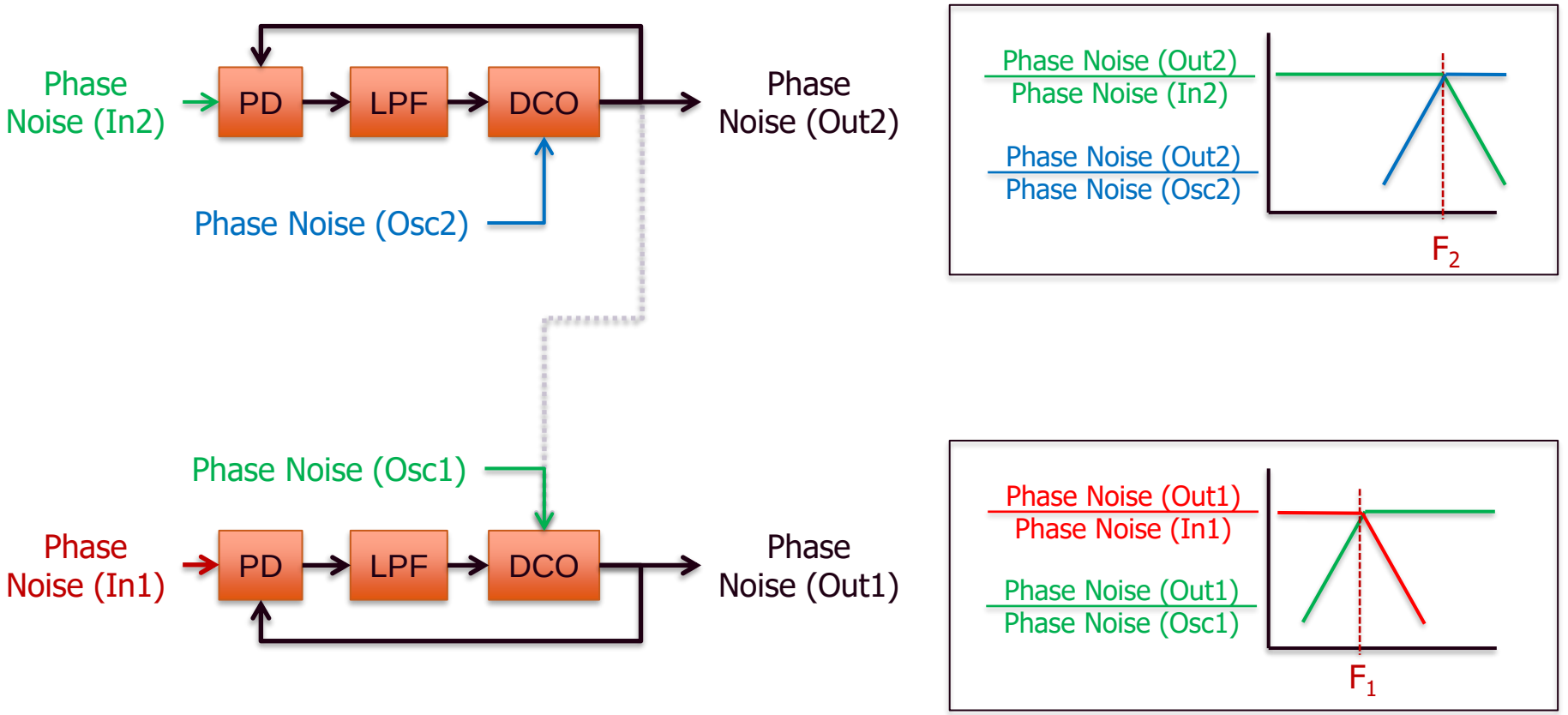
$D =$ frequency drift rate (constant)



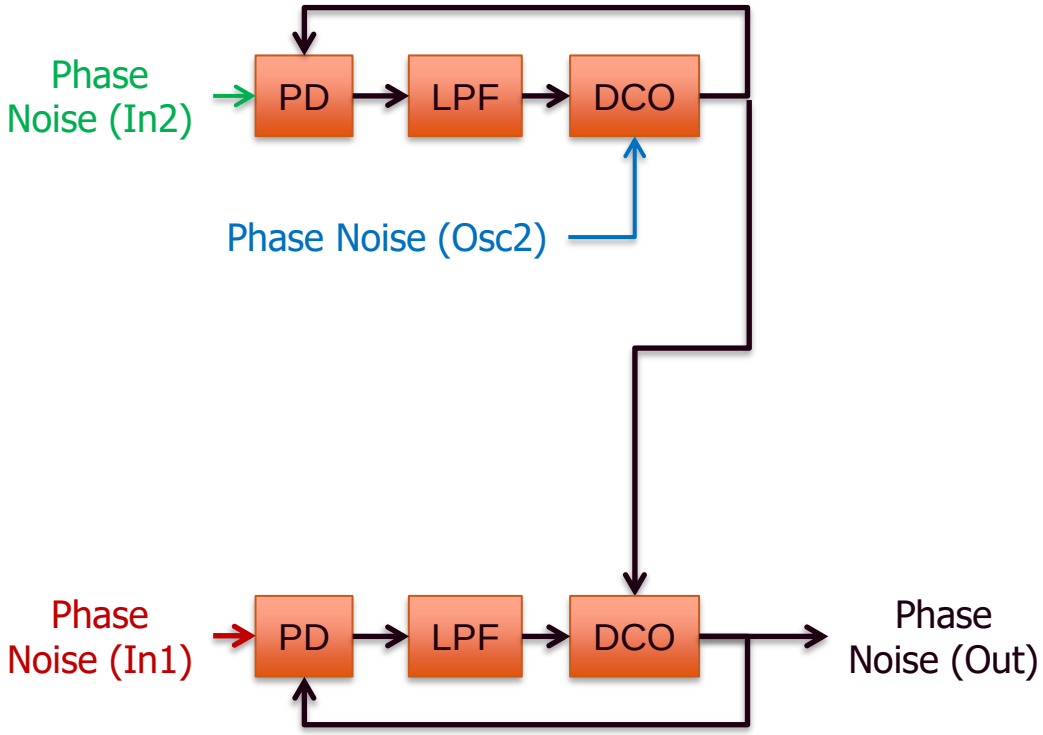
PHASE LOCKED LOOPS (PLL)

CLOCK COMBINING

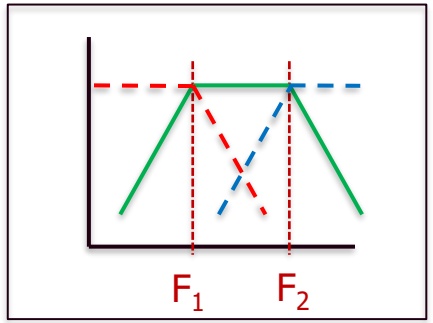
COMBINING TWO PLLS



TWO PLLS: RESPONSE TO INJECTED NOISE

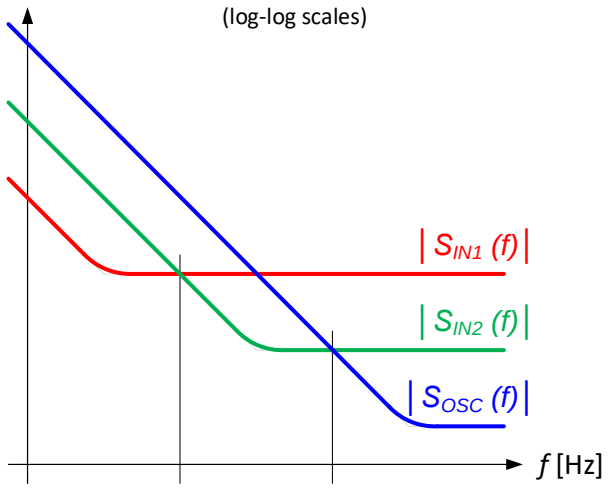


Band-pass filter for In2 Noise to Out

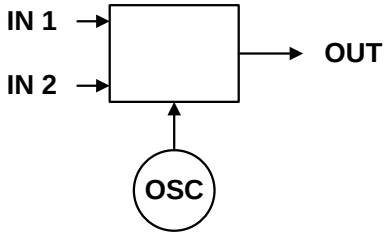


TWO PLLS: SPECTRAL DENSITIES

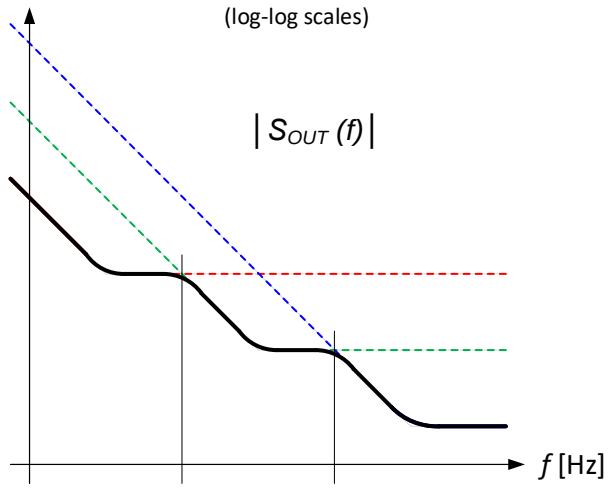
Three spectral densities (phase-time) …



… combined by the 2-input PLL, …

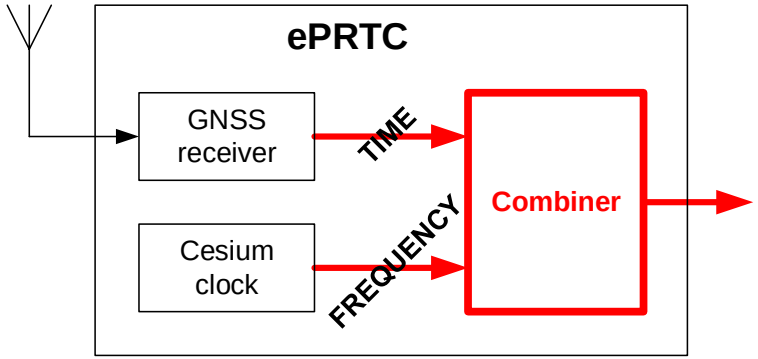


… result in this out spectral density:

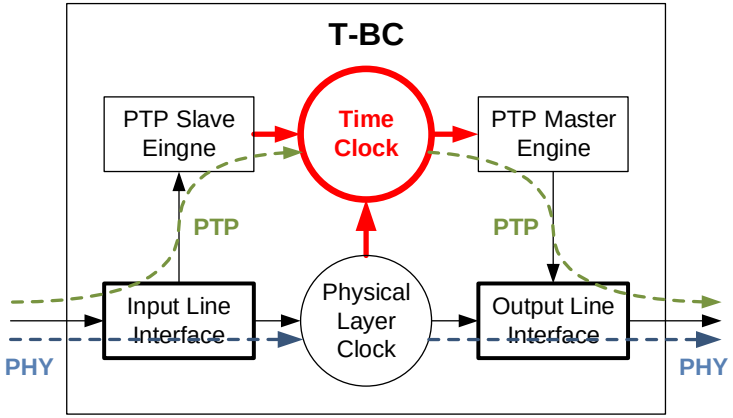


TWO PLLS: APPLICATIONS

- **GNSS & Cesium clock** in enhanced Primary Reference Time Clocks (ePRTC)

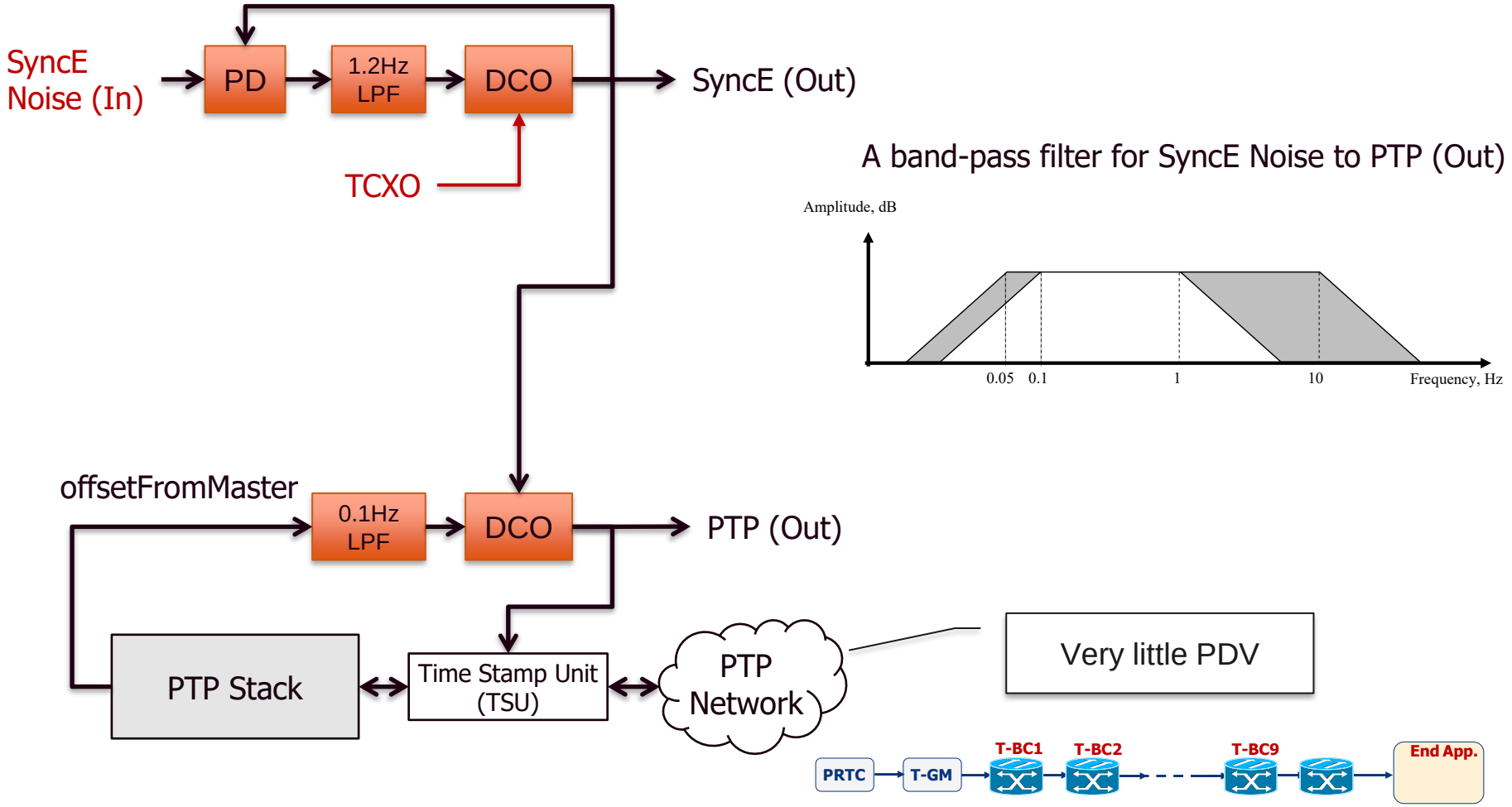


- **PTP & SyncE** in boundary clocks (T-BC) and slave clocks (T-TSC)



Note: PLL with 2 inputs is not the only way of combining 2 references

G.8273.2 T-BC: RESPONSE TO INJECTED SYNCE NOISE



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Timing is the heartbeat of the system