WSTS 2022

Calnex

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‘Hidden Challenges’: Sync Impact of New Networks

Making it Work…

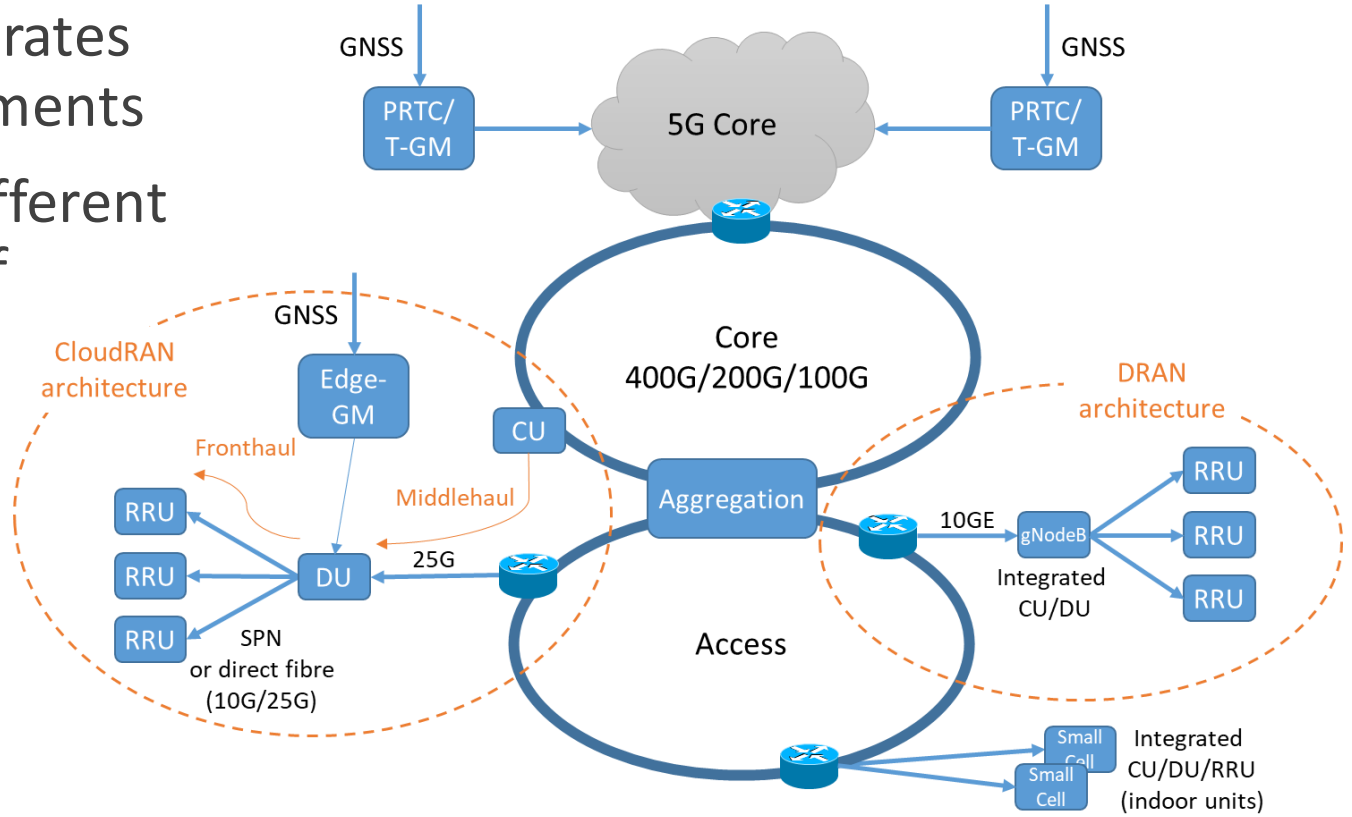
- Multiple applications are now truly using **real-world** network synchronization
- This means timing issues can be **the** blocker to deployment
- Standards help, but…
- There are always some specifics that must be dealt with **in practice**

- **As new technologies are deployed, there can be hidden challenges waiting…**

5G backhaul – Knowns and Unknowns?

- Well understood that introducing new rates adds to development and test requirements
- Common themes for time and sync: different lane speeds, encoding types, impact of latency for FEC implementations……

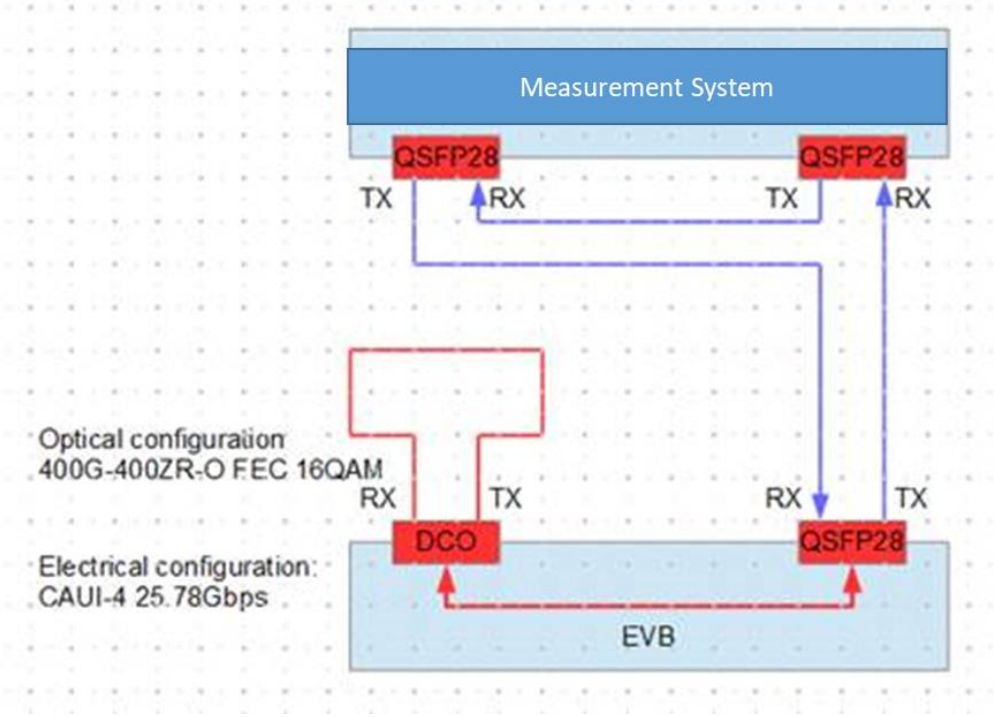
……What about optics???



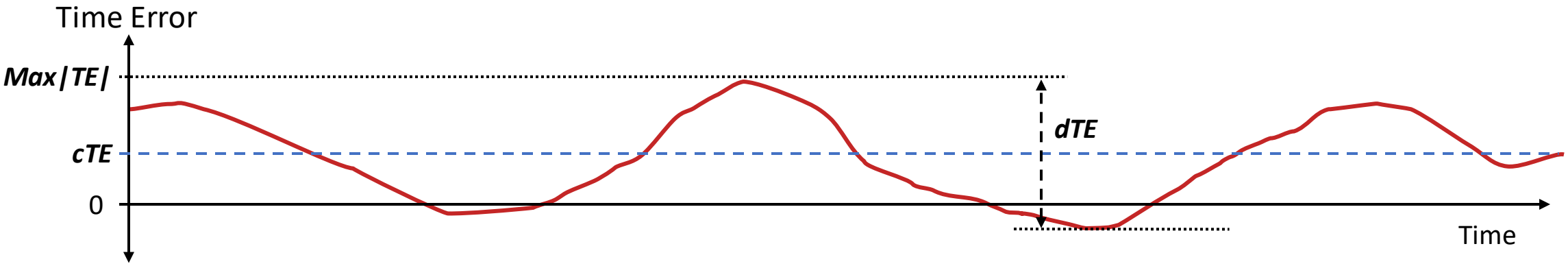
(First reported ITSF Brighton 2021) Investigations: Impact of Optics on 'complete' device timing performance

- Preliminary testing using known performance 'golden' optics and eval board loopback

(note: worst case impact of NRZ optics on latency/timing measurements is in the picoseconds)



Preliminary results – timing impact of PAM4 optics



	50G PAM4 (SR)	400G PAM4 (LR8)	400G PAM4 (FR8)	400G PAM4 (FR4)
Typical Latency (ns)	67.81	65.25	64.67	73.77
Run to run Latency variation (ns)	+/-0.01	+/-0.01	+/-0.01	+/-0.01

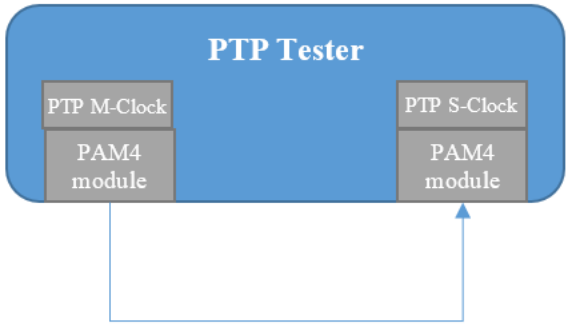
- PAM4 optics introduce an additional challenge when using with devices targeting **ITU-T Class-C or Class-D specifications**
- For **Class-D,** optics become a significant contributing factor to 'device' performance:

  Unmatched optics on a link *could* affect cTE in the range of ≈5ns

Latest Investigations:

- Detailed testing now in progress using more direct latency testing methodology
- Precision timestamped PTP packets used
- HOT OFF THE PRESS: findings submitted to ITU-T Q13 last week…

Question(s):	13	**Meeting, date:**	E-meeting, 3rd – 6th May 2022
Study Group:	15 **Working Party:**	3	**Intended type of document** (R-C-TD): WD13-xx
Source:	Calnex		
Title:	Results of latency measurements of PAM4 optical modules		



Baseline measurement: 50G and 400G electrical DAC cables

Delta measured vs 50G SR,
400G SR8,
400G LR8 and
400G FR4 optics

Figure 1: Single device test configuration

Latest Investigations:

- Multiple vendors, multiple modules measured
- Some reason for concern in all metrics

Test Case	Vendor	Mean Latency (ns)	Reset-to-reset Variation (ns)	Packet-to-packet Variaton (ns)
50G SR	Vendor A	68.0	2.1	<1
50G SR	Vendor B	60.9	1.5	<1
400G SR8	Vendor A	70.9	3.0	<1
400G LR8	Vendor A	64.8	3.5	<1
400G FR4	Vendor A	73.8	1.2	<1
400G FR4	Vendor C	74.9	1.4	2.5

Latest Investigations (cont.):

- **ASYMMETRY is the time killer…**
- Simpler 25G NRZ optics may have a total latency of ~1ns. Therefore, any time error resulting from assumptions about the Tx/Rx latency split will be no more than 100-200ps.
- With PAM4 optics, the total latency is much larger, however, and the assumption that the Tx and Rx latency is the same can introduce significant time error…

Test Case	Asymmetry	Total Latency (ns)	Tx Latency (ns)	Rx Latency (ns)
400G SR8	Measured asymmetry	70.9	26.0	44.9
400G SR8	Assumed 50/50	70.9	35.45	35.45
400G SR8 Error	-		**-9.45**	**+9.45**

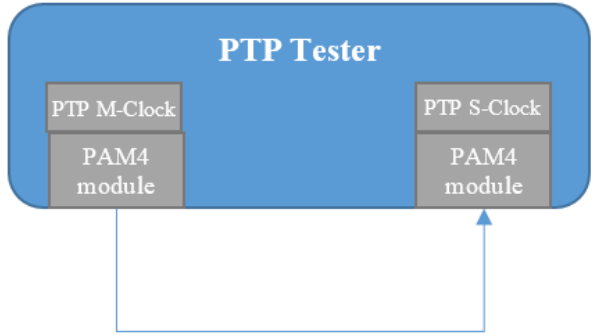
Optical module latency: Next Steps

1. More investigation – biggest delay/variation contributions?:
   - Specific chipsets
   - Rx Clock Recovery
   - Line coding, FEC…
2. Short term, very close management of deployment conditions required?:
   - Some vendors already investigating ‘matched optics’
3. Investigate improvements to ‘next-gen’ of optical modules:
   - Performance improvements
   - ‘e1pps’ or other methods to compensate for run-to-run variation ‘on-the-fly’

What about a capability to measure Tx/Rx latency of modules…

Verifying Optical Modules: Summary

- As shown previously, total latency through a pair of optical modules can be characterised today, using systems with performance timestamping



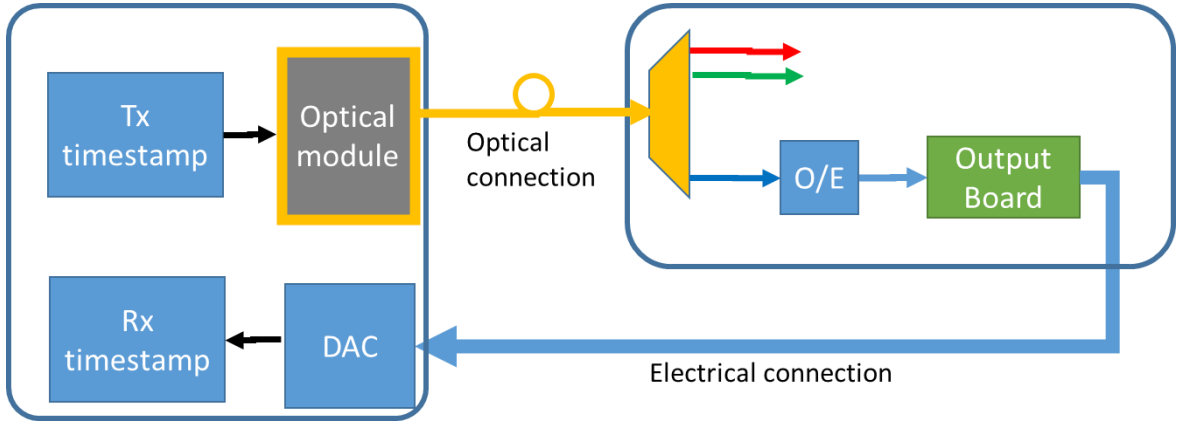
- However, if we do not know the Tx/Rx split, we could end up with a large asymmetry (>10ns) which is a major issue for e.g. PTP accuracy.

- Knowing Tx/Rx behaviour of modules could allow compensation - or at least allowance – in systems

- Often little/no information from Vendors about Tx/Rx latency.
  - Totally reasonable, as in the past, no applications suffered from latency in us/ns ranges

Verifying Optical Modules: A way forward?

- Solution could be created combining elements with known performance (i.e. error contributions in low ns range)
- Rx latency could be derived from measurements of Total Latency and Tx latency.



Summary and Conclusions

- It is known and accepted that new technology iterations pose challenges when meeting sync performance requirements – the industry as a whole has good reason to believe these can be overcome!
- **The concept of optical modules as a significant factor is new – and not all required information is available**
- Talking and sharing experience will help get ahead of these issues
- Some pending challenges are ready to act on now – we are interested to progress these discussions!

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