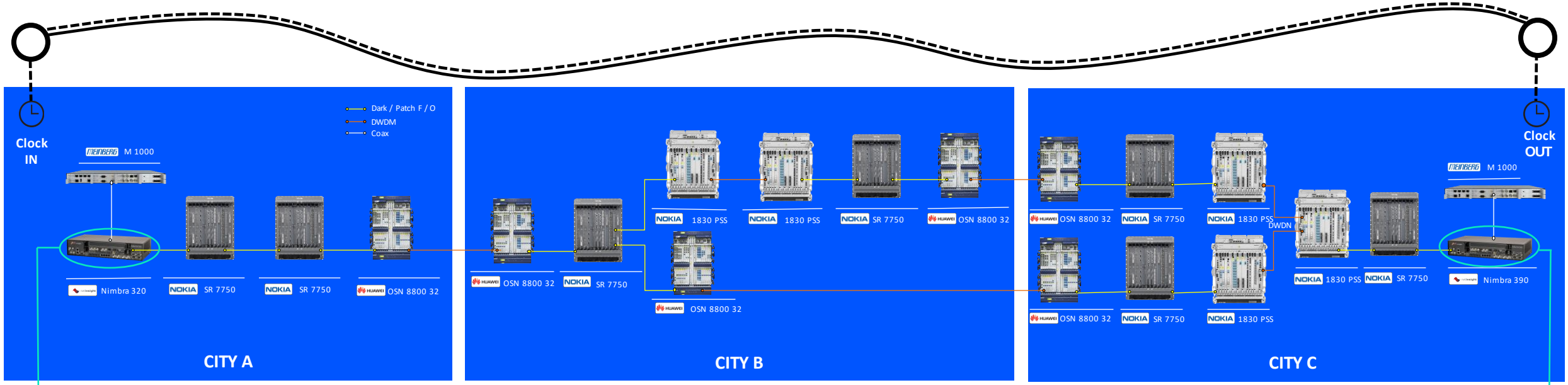
Challenges of timing over packet network

- Full timing support for PTP has proven challenging to achieve for operators
  - Upgrade of WAN DWDM & MPLS equipment not always feasible
- Partial timing support for PTP has not been sufficient
  - Operators faced severe performance issues
- No timing support
  - Pro: Can run over existing equipment
  - Con: Requires handling full timing jitter
- No timing support hybrid – intermediary nodes
  - A set of nodes operating over network sections with no timing support
  - Jitter reduction in each intermediary and final nodes
- Assymmetric delays needs compensation
  - No timing support (with or without intermediary nodes) will be exposed to uncompensated network delay
  - Once jitter properly managed, assymmetric delay compensation is manageable

Use case, Time Transfer over MPLS and Transmission

~1200 km Distance ***11/14 Hop*** ***< 170 ns Accuracy***



Nimbra Time Node

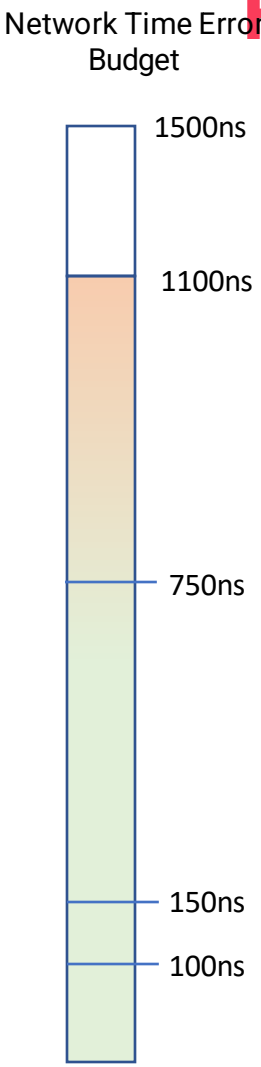
Asymmetry and PDV solved with Precision TimeNet

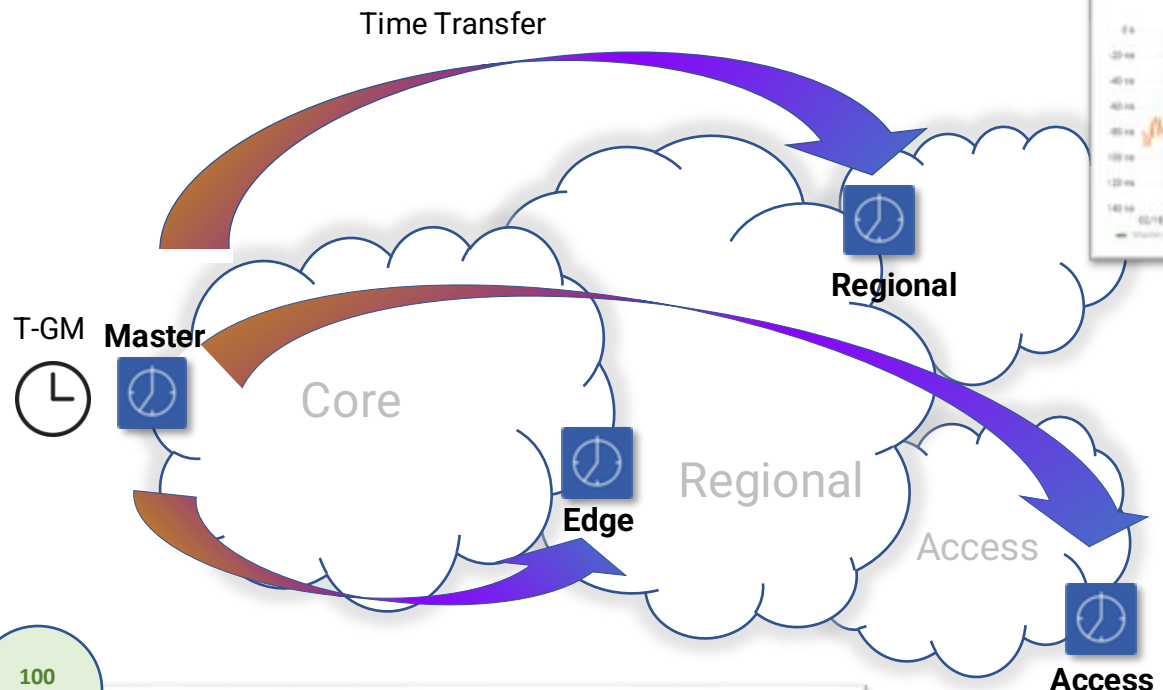
Nimbra Time Node

Türk Telekom
Değerli Hissettirir

netinsight

Proof of Concept performance in operator network



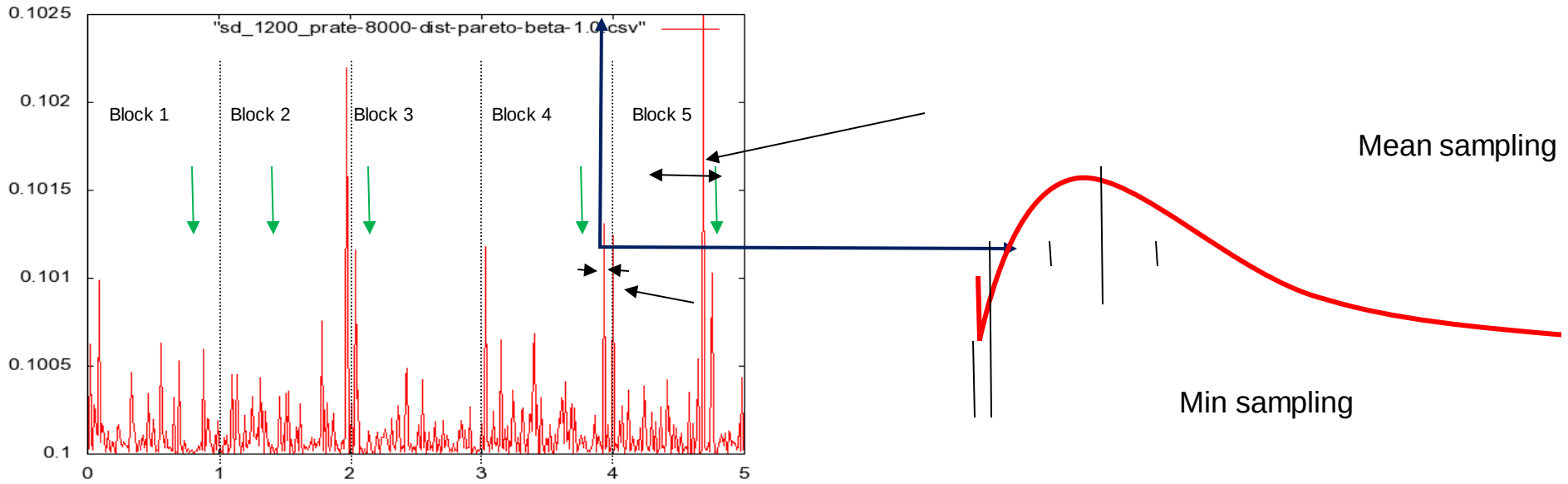


Regional – within 150 ns max|TE|

Access, leased line – on 750 ns max|TE|
Working on it

Edge of the core network – within 100 ns max|TE|

Min delay estimation - ”Lucky packet”

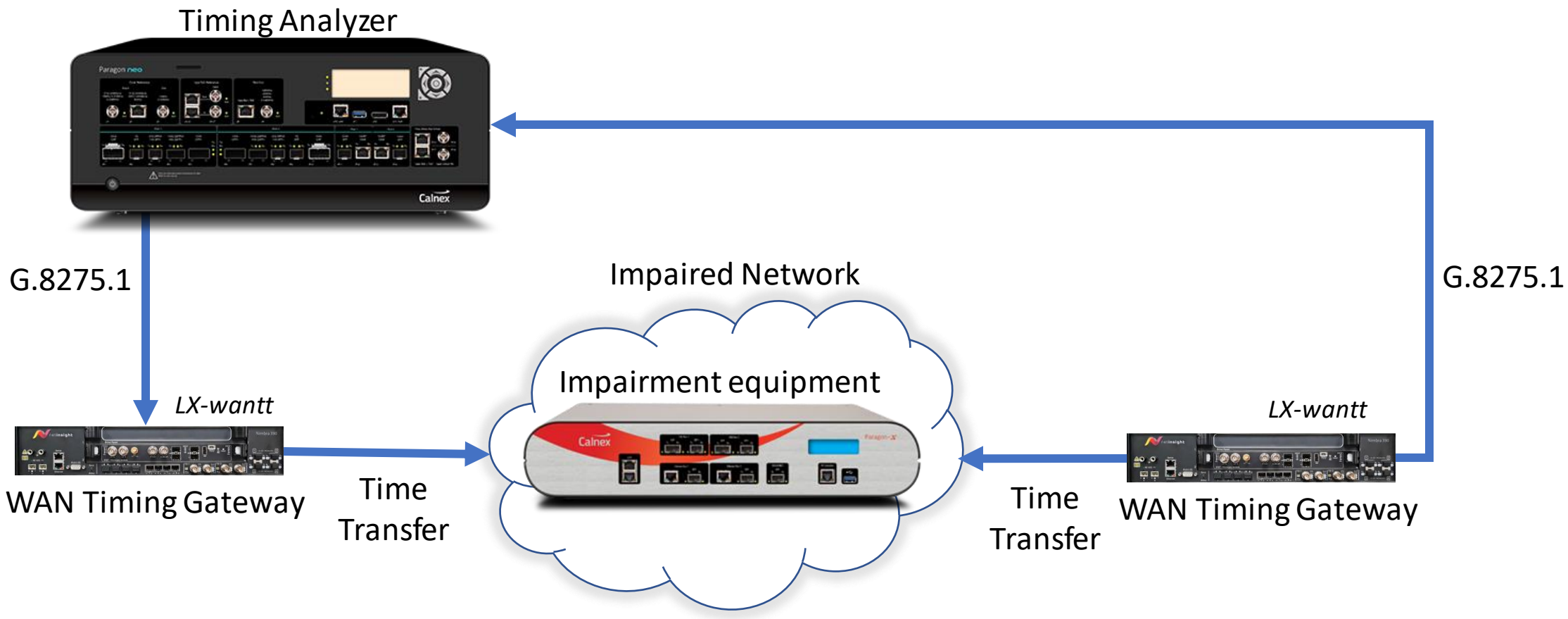


- Packet Delay variations as time-series has some distribution
- The actual distribution has some actual minmum delay
- Approximation to minimum delay found using minimum of a block of delay estimates
- Much of actual delay variation, mean is removed, to be replaced with that of the variations of the new min distribution
- Block size significant to good surpession => drives packet rate up

Network Impairment – a scale down approach

- Full G.8261 VI setup is complex
- Packet load vs. PDV profiles
  - Particular packet load patterns create particular PDV patterns
- PDV properties
  - True Minimum delay
  - Average delay
  - RMS
  - Average min delay – “lucky packet” (0.1 % percentile)
  - Peak-to-peak
- Average and variation key components for clock recovery
  - Unfiltered or min delay variants key focus => impairment and measure of these

Test setup 1

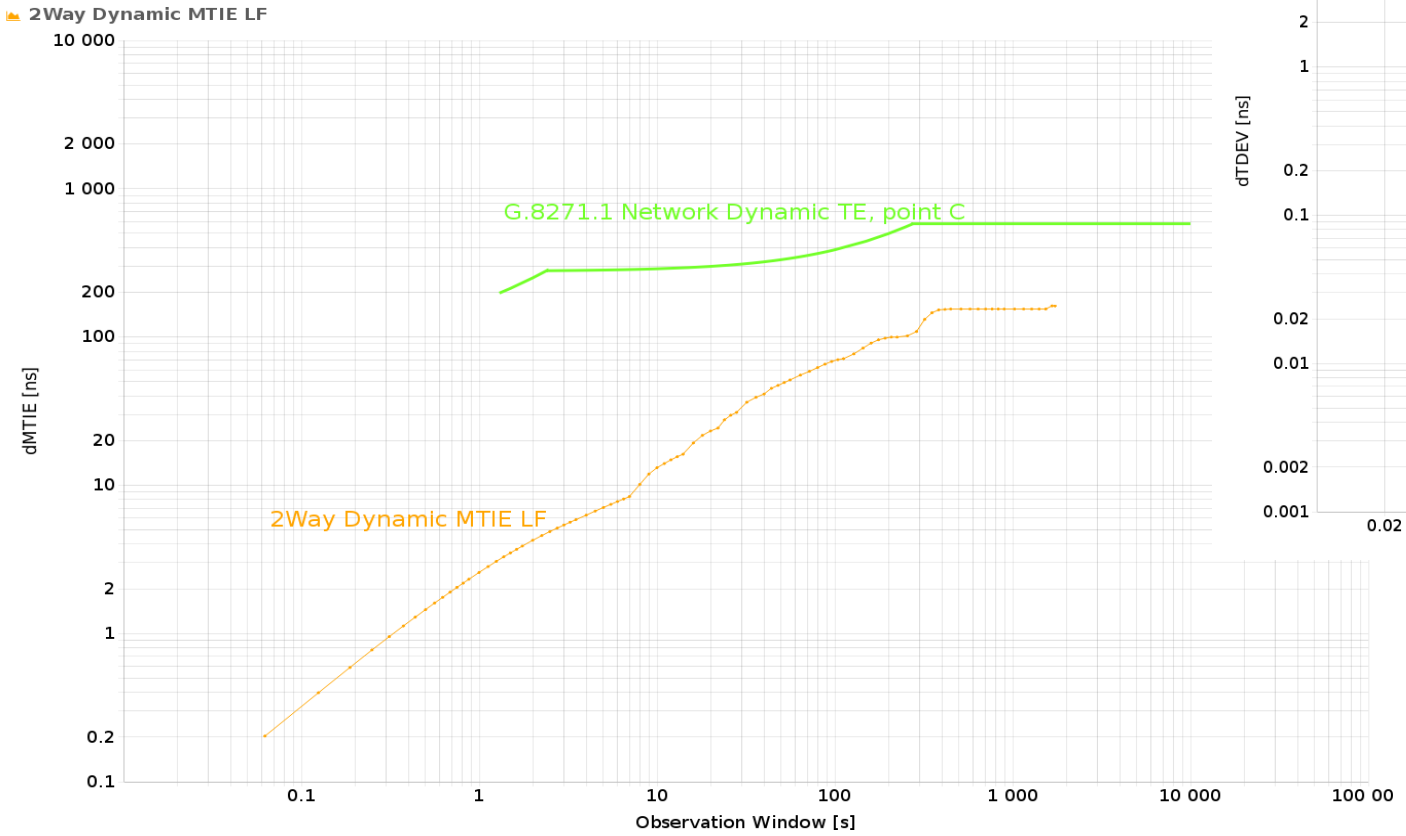

Timing Analyzer
G.8275.1
Impaired Network
Impairment equipment
G.8275.1
LX-wantt
LX-wantt
WAN Timing Gateway
Time Transfer
Time Transfer
WAN Timing Gateway

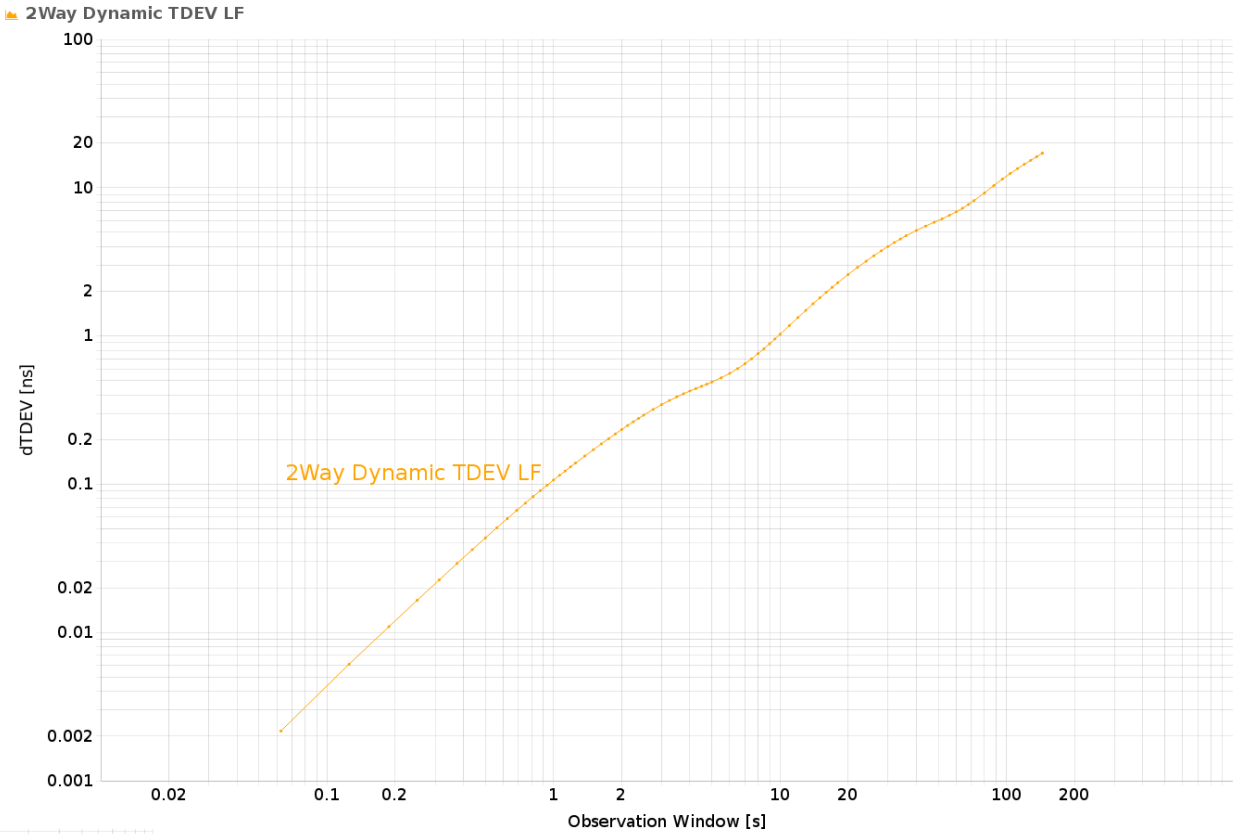
Baseline measurement

100 us static delay

100 Mb/s – 8000 packets/s

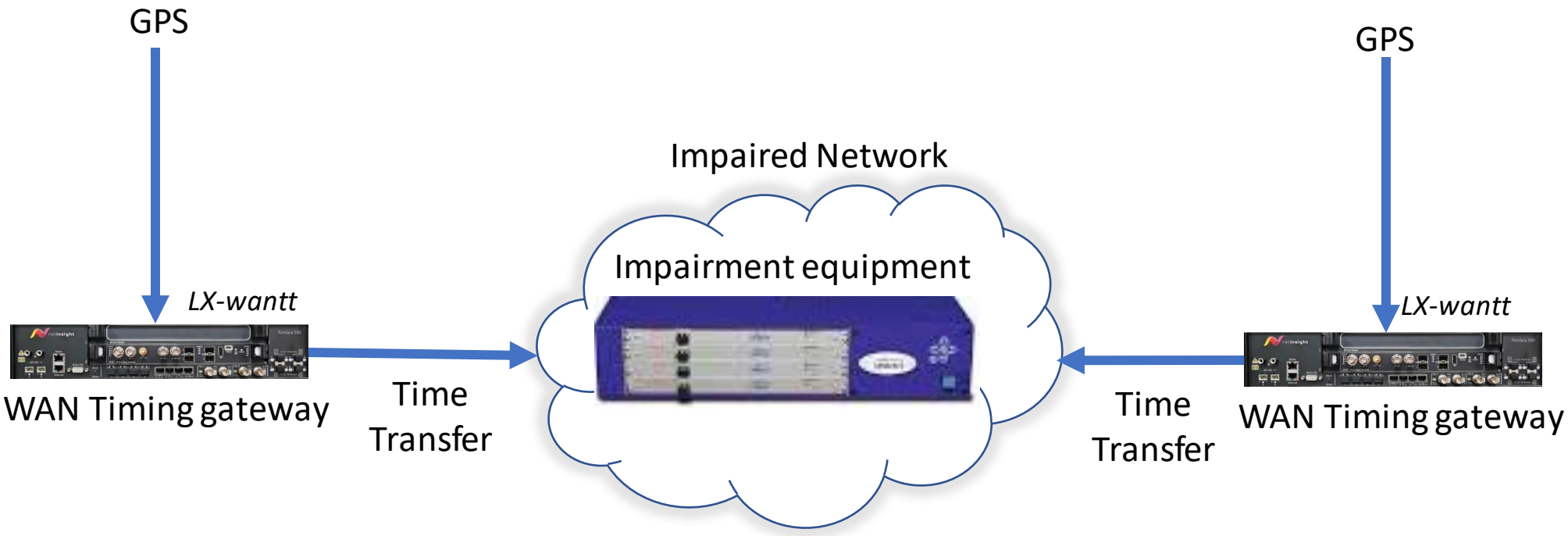
Calnex Paragon NEO noise is low





Test setup 2

Alternative setup using internal statistics collection



A min value measurement

A->B delay	B->A delay	0.1 % percentile	RMS	Peak-to-peak	0.1% / p-t-p
100 us	100 us	77 ns	49 ns	409 ns	0.188 264
+ 100 us triangle	+ 100 us triangle	91 ns	29 215 ns	100 194 ns	0.000 908
+ 100 us Poisson	+ 100 us Poisson	302 ns	21 526 ns	100 545 ns	0.003 004
+ 200 us Poisson	+ 200 us Poisson	581 ns	43 003 ns	200 999 ns	0.002 891
+ 400 us Poisson	+ 400 us Poisson	522 ns	85 878 ns	401 218 ns	0.001 301
+ 800 us Poisson	+ 800 us Poisson	1 083 ns	171 800 ns	802 473 ns	0.001 350

Measurement done using 100 Mb/s 8000 packets/s rate

For these measurements Round-Trip-Time remained essentially unchanged at 200 us

For these measurements Time Error was low

Variation of produced output increase roughly in proportion to p-t-p range

Measurement consistent with expected result – significant reduction of variation

Conclusions

- Challenges and background of study presented
- Challenges of measurement setup discussed
- Test setups conducted
- Significant reduction of variation measured and verified
- Real life challenges can severly affect measurement campaign results
- Many thanks to Calnex and their supportive staff