

Software Defined Timing: The Synchronization Solution for Data Centers



Francisco Girela

www.sevensols.com

Summary

- Introduction
- White Rabbit technology integrated in third parties towards scalability.
- Software defined timing: High Accuracy Timing IP core (HATI)
 - HATI 1G
 - HATI 10G
 - HATI integration example



Introduction

INDUSTRIAL AUTOMATION

Alveo—An FPGA Board for the Cloud and Data Center

Xilinx's Alveo goes beyond machine-learning applications, bringing high-end FPGAs to the enterprise. The high-end U250 delivers 33.3 INT8 TOPS.

Facebook explores building its own ASICs and FPGAs

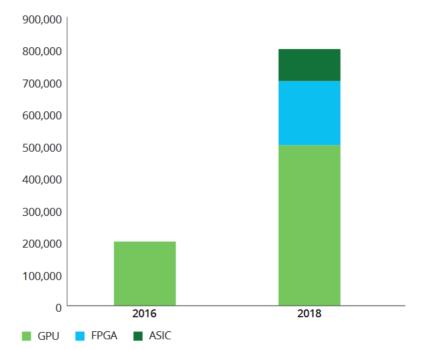
HOME > NEWS > SOUTH EAST ASIA

SK Telecom deploys Xilinx FPGAs in its data center

COMPANIES > MICROSOFT

Why Microsoft Has Bet on FPGAs to Infuse Its Cloud With

Figure 13. Annual minimum sales of ML chips in global data centers (units)



Source: Deloitte Global estimates, 2017, based on publicly available information. See endnotes for full methodology.



White Rabbit technology



White Rabbit technology

White Rabbit (WR) is a technology born at CERN which achieves sub-nanosecond accuracy in Ethernet based networks. It allows easy deployments of scalable and reliable networks with high accuracy synchronization requirements.





White Rabbit technology

- +10 years of expertise synchronizing large scientific facilities: **G S i i i Fermilab**
 - CERN, GSI, Fermilab, ...
- Validated by National Metrology Institutes: NIST, NPL, PTB, OP, VSL, ROA, VTT, RISE, ...
- New PTP High Accuracy profile to be released is based on the • pre-standard approach White Rabbit.



White Rabbit technology



Easy to integrate within existing infrastructures (Ethernet, PTPv2).



Scalable

to long distances & high number of nodes. It supports tree topologies and daisy-chain configurations



Deterministic and highly accurate This allows saving engineering and equipment costs to achieve a global target time budget.



Dependable It reduces vulnerabilities to spoofing or GPS jamming. Up to 100 km links without on site calibration.



Cost-effective

It compensates dynamically link asymmetries and temperature changes. Easy to deploy, precalibration.



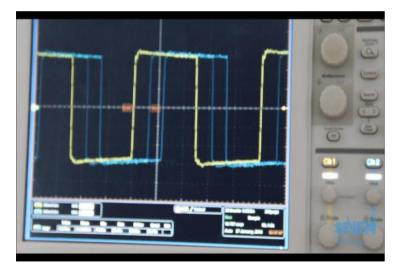
Facilitates new services

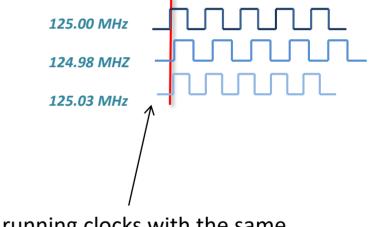
Positioning, High Frequency Trading, Time as a Service



White Rabbit technology: Syntonization

- To reach subnanosecond synchronization, distributing the same clock through the network is needed.
- Syntonization: local clock tuning based on a measure of the error between two clocks. In White Rabbit, the external clock and the internal reference are compared.





Free running clocks with the same nominal frequency are not accurate enough for accurate time transfer



White Rabbit technology: Syntonization

L1 syntonization is used as a customized version of **Sync-E** to transmit the clock over the optical links. It uses local VCXO to syntonize the local clock to the recovered clock from the link (Slave role).



White Rabbit **requires specific clock circuitry** to perform the syntonization and ensure accurate time synchronization.

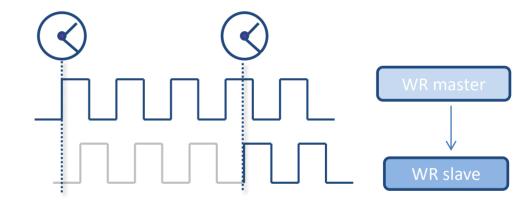


White Rabbit technology: Ultra-accurate timestamp

Synchronization: L1 syntonization & PTP (IEEE-1588v2)

White Rabbit measures the offset between devices, taking into account the link asymmetry and dynamic variations because of weather conditions using **picosecond level accurate timestamps**.

Timestamp generation based on frequencymixingtechniques:Clockphasemeasurements

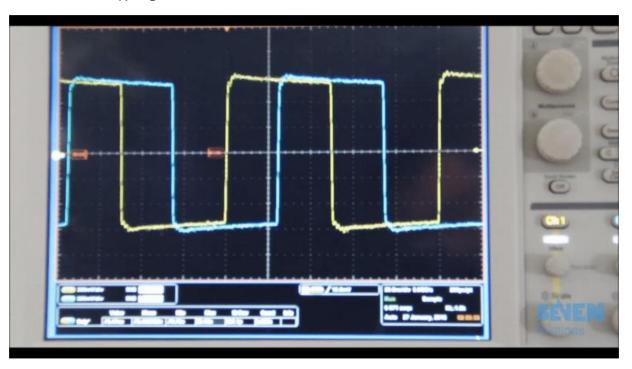


The timestamps are capable of measuring time differences between two digital clock signals with very fine resolution (picosecond) and they are used to adjust the received and generated clock offsets.



White Rabbit technology: Synchronization

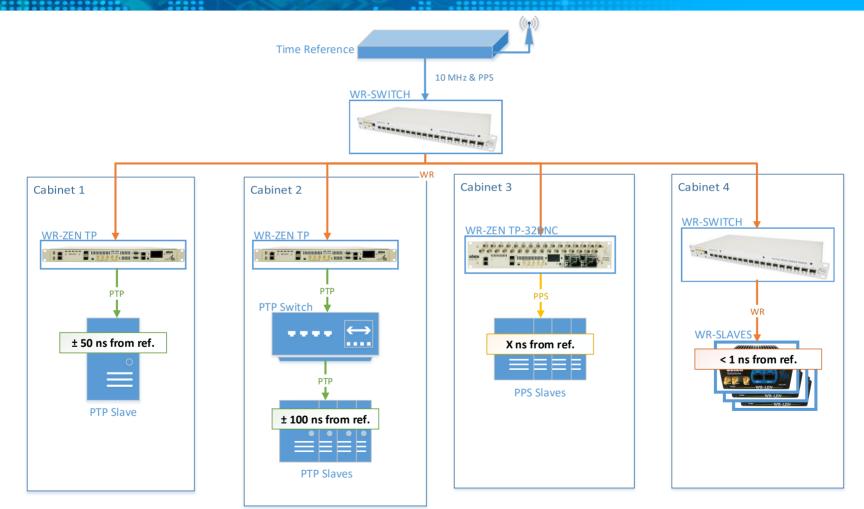
White Rabbit uses the information collected by the exchange of timestamped packets for correcting the constant offset between nodes $(b_A \neq b_B)$



The information from the calibration is also important for compensating the static offset between nodes.



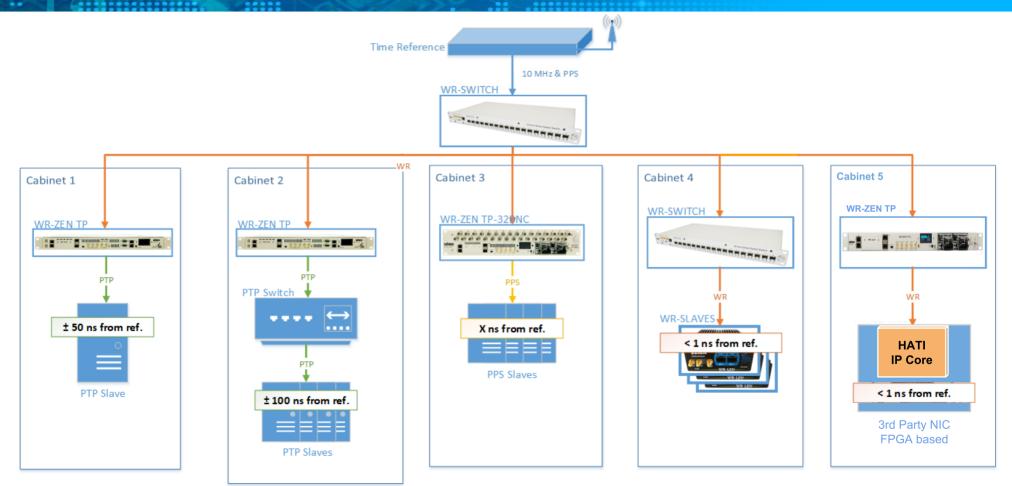
White Rabbit technology: Interoperability



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Software defined timing: High Accuracy Timing IP core





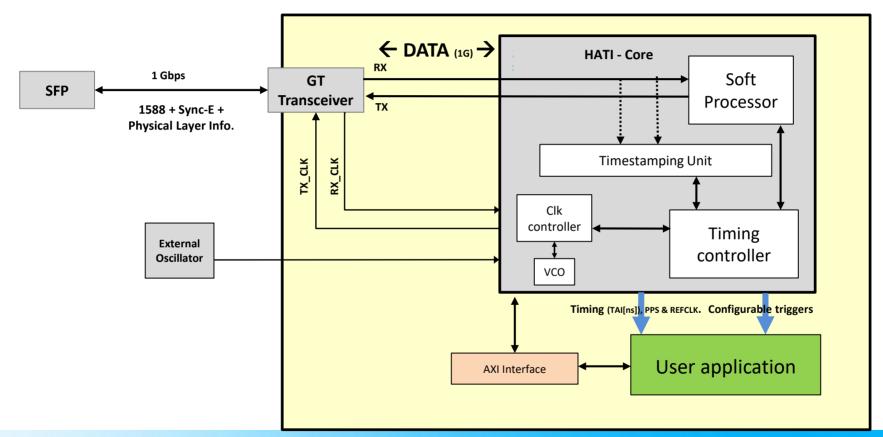
Software based solution:

- Based on White Rabbit technology (PTP v2.1 HA adaptable).
- FPGA IP core.
- **1G/10G** supported. 25G/40G in scope.
- Several Xilinx FPGA families supported.
- Specific clock circuitry not required.
- High resolution **timestamps**.
- **Sub-nanosecond** synchronization accuracy.
- Very precise **frequency distribution**.
- **Dynamic compensation** of asymmetries caused by **weather conditions**.
- Minimal data bandwidth consumption.
- Easily integrable.
- Distance range over **80 km without calibration** using precalibrated optics.
- **DWDM** compatible.



HATI 1G: Architecture

HATI template architecture: Xilinx FPGA (Family-7)

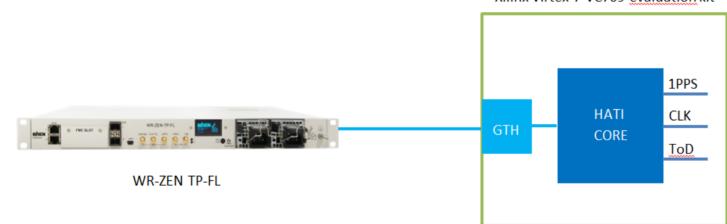


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HATI 1G: Results

Example of HATI-1G performance: Test over 20 km of fiber during 84 hours.



Xilinx Virtex-7 VC709 evaluation kit



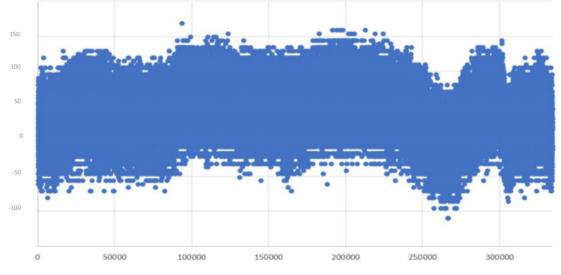
Example of HATI-1G performance: Test over 20 km of fiber during 84 hours.

Max-Min (ps)	280,66	
Mean (ps)	/lean (ps) 52,54	
Std. Dev. (ps)	43,1595261	

HATI 1G: Results



It ensures an error below 300ps



PPS offset

Figure 1: Long-term PPS offset measurement.

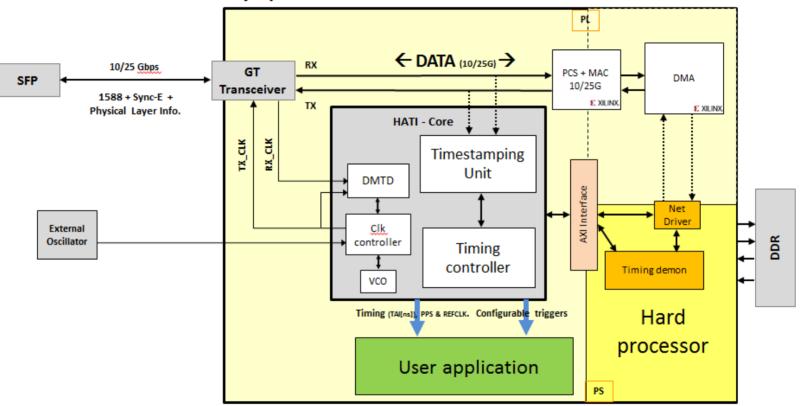


HATI 10G: Architecture

HATI template architecture:

Zynq Achitecture

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HATI 10G: External clock cleaner

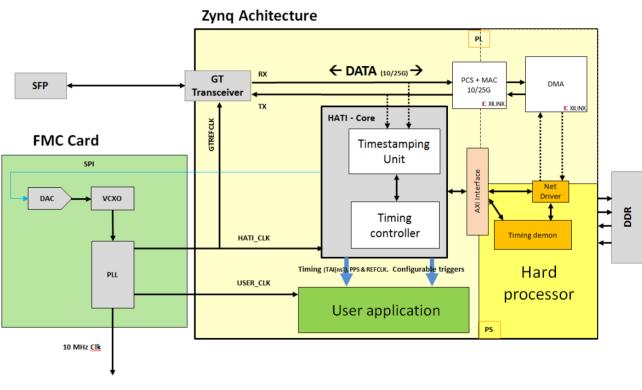
Optional: For frequency dissemination applications requiring low jitter, the HATI core can accept an external PLL to clean the clock signal from the FPGA.

Example of FMC cards with external clocking circuitry



Stability with and without external hardware:

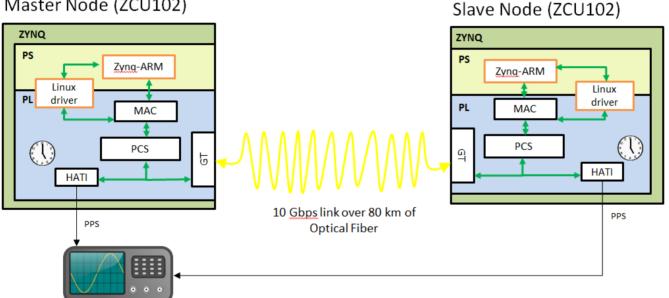
	Std. deviation	Peak to peak
External HW	8.03 ps	78.45 ps
Without Ext. HW	19.25 ps	137.12 ps

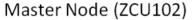




HATI 10G: Results

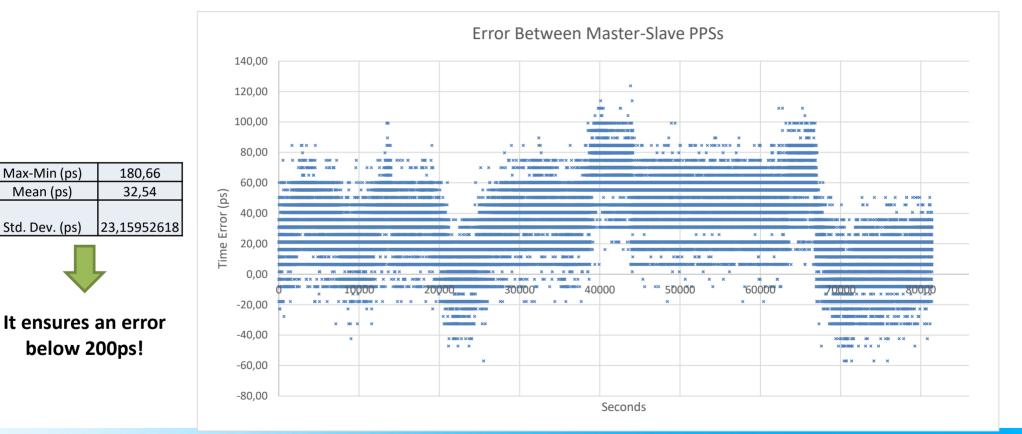
Example of HATI performance: Preliminary test over 80 km of fiber during 24 hours.







HATI performance: Non-temperature controlled test over 80 km of fiber during 24 hours.





Max-Min (ps)

Mean (ps)

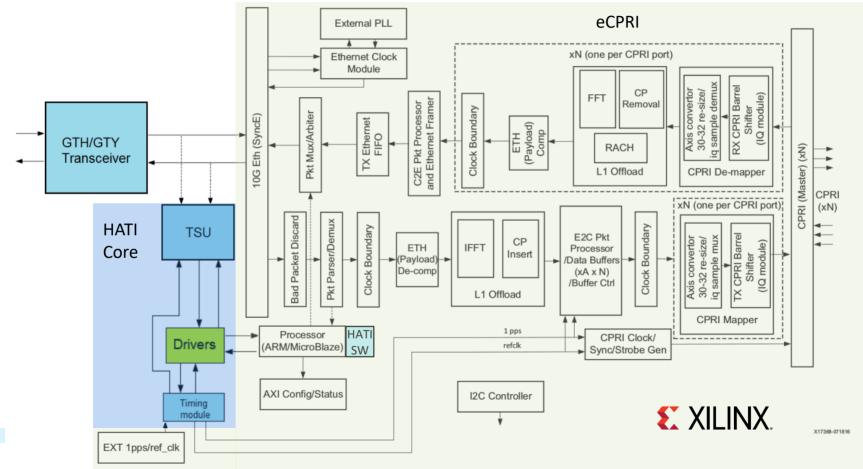
Std. Dev. (ps)

below 200ps!

HATI 10G: Results.

HATI integration example: Xilinx eCPRI.

Example of HATI integration: eCPRI Gateway design (Xilinx).



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