Designing for high-accuracy time transfer

Calnex
Insight and Innovation

TE_L – the new metric for Class D clocks

- Each Class C or D boundary clock contains a 0.1Hz low-pass filter to smooth out noise at its input. Therefore only low-frequency wander propagates along the chain of clocks
- TE_L (low-pass filtered Time Error) is therefore representative of the amount of time error a device generates that will propagate along the chain and affect the output time

G.8273.2: T-BC Classes

Parameter	Conditions	Class A	Class B	Class C	Class D
Max | TE |	Unfiltered, 1000s	100ns	70ns	30ns	FFS (15ns proposed)
Max | TE_L |	0.1Hz low-pass filter 1000s measurement	–	–	–	5ns
cTE	Averaged over 1000s	50ns	20ns	10ns	FFS (4ns proposed)
dTE_L MTIE	0.1Hz low-pass filter Const. temp., 1000s	40ns	40ns	10ns	FFS (3ns proposed)
	0.1Hz low-pass filter Var. temp., 10,000s	40ns	40ns	FFS	FFS
dTE_L TDEV	0.1Hz low-pass filter Const. temp., 1000s	4ns	4ns	2ns	FFS (1ns proposed)
dTE_H	0.1Hz high-pass filter Const. temp., 1000s	70ns	70ns	FFS	FFS (15ns proposed)

FFS – For Further Study

High accuracy by design

Low variation in Time Error achieved through high accuracy during design

- Eliminate whole clock cycle variation
- Minimize sub clock cycle variation

The techniques employed by Calnex to create high-accuracy test solutions can be equally applied to all designs of devices that are required to deliver high-accuracy time transfer.

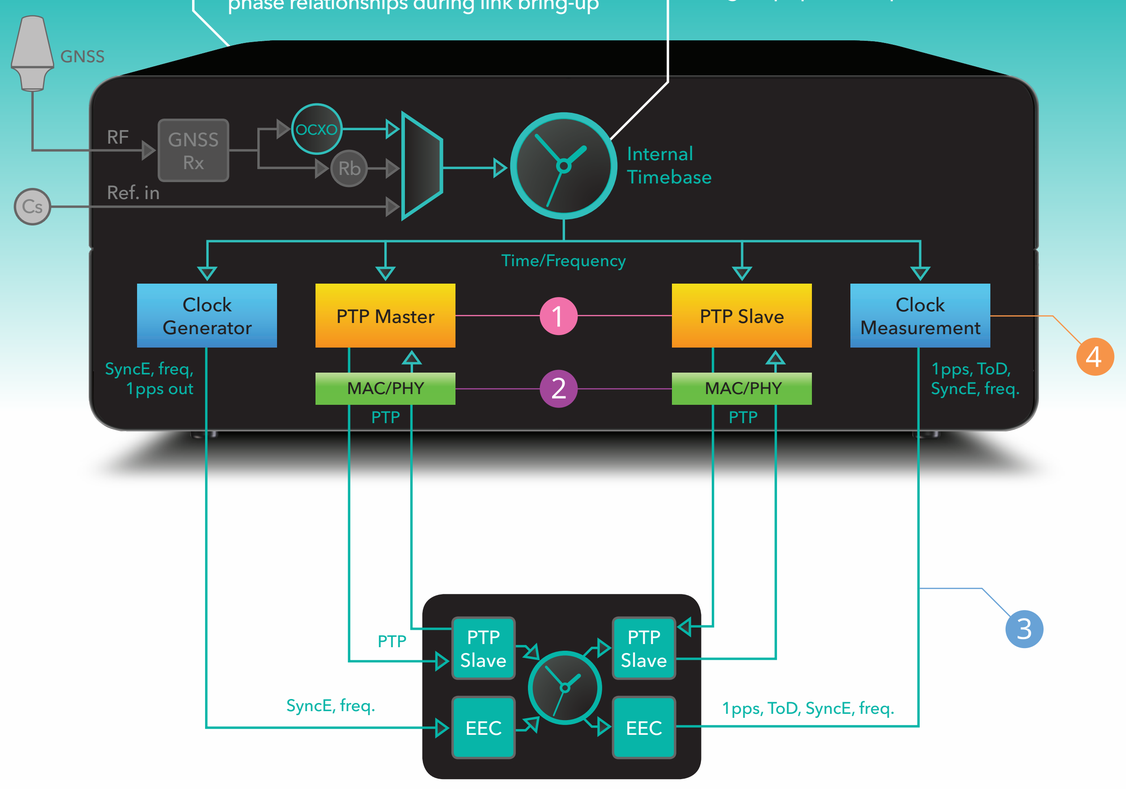
These are reference options that might not be required for all tests, hence greyed out

ACHIEVING REPEATABLE PATH DELAYS

- Eliminate clock boundary crossing wherever possible
- Maintain a known phase relationship between critical clocks
- Design in ability to detect/correct wrong phase relationships during link bring-up

CLOCKING

- Use low phase noise clock sources
- Minimize clock skew variation
- Minimize clock jitter in FPGAs/ASICs
- Utilize clock phase shifting features e.g. 20ps phase steps



T-BC under test

1

- Lock down critical paths in FPGAs to avoid changes from release to release
- Use Correction Field for sub-nanosecond resolution on all timestamps

2

Maintain control of critical IP e.g. MAC and PCS layer, to ensure:

- Accurate time-stamping of Rx packets
- Control of Tx and Rx path delays

3

Provide accurate control of cable compensation and threshold levels:

- Cable compensation to picosecond resolution
- 1pps threshold voltage to 10mV resolution

4

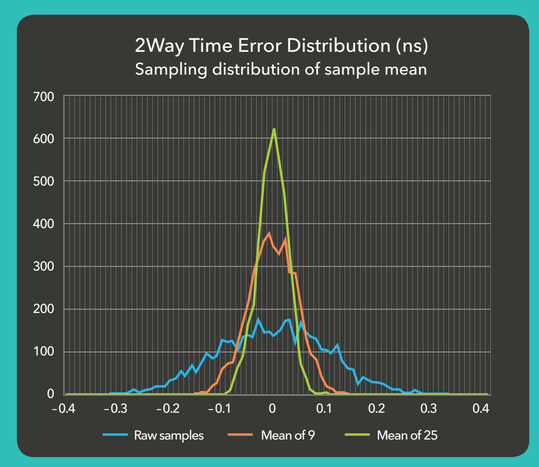
1pps:

- Treat 1pps as a GHz signal for high-precision phase alignment
- Minimize skew on 1pps (or any signals carrying phase) by using low skew fanout buffers (<20ps)

High accuracy by calibration

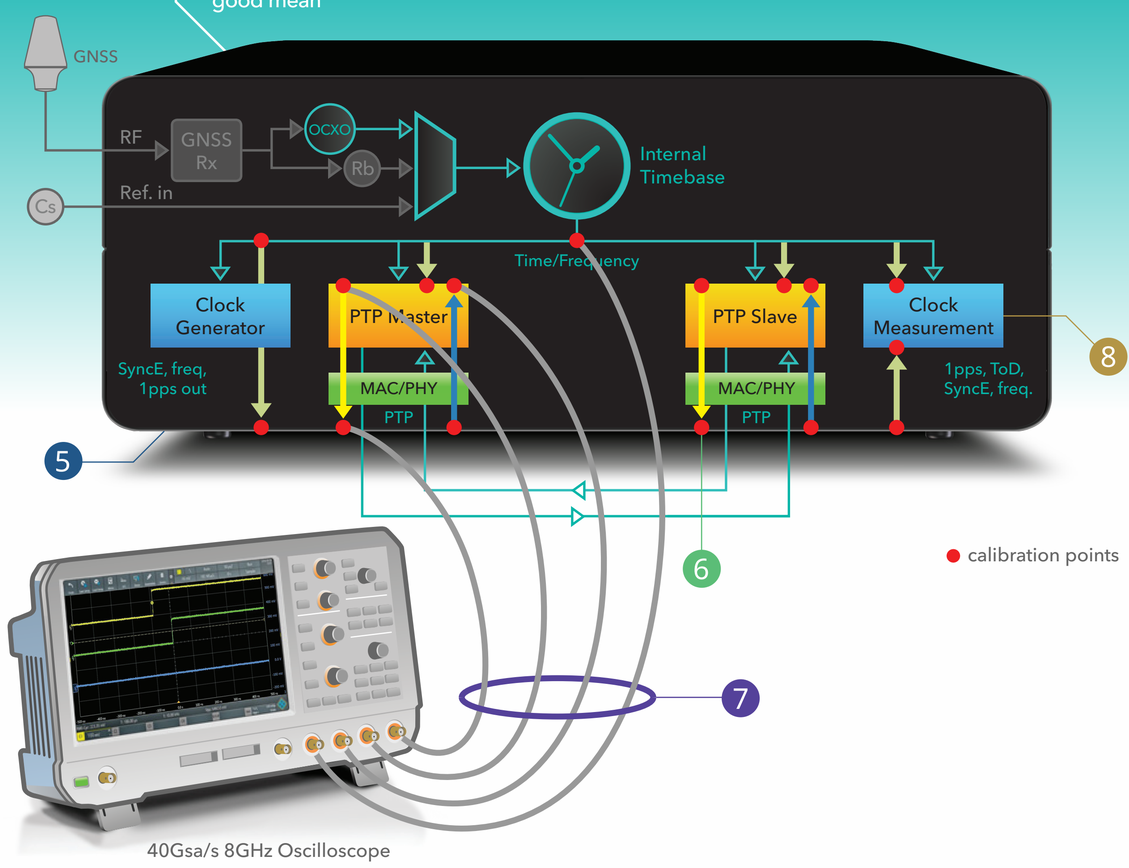
Absolute accuracy achieved by accurate calibration

- Accurately remove all probe delays
- Repeat calibration many times to achieve the best mean of results



SCRIPTING CALIBRATION

- Use scripts to automate configuration of the device being calibrated and the high-accuracy test equipment
- Repeat calibration many times to give a good statistical mean. The bigger the spread, the more runs required to get a good mean



40Gsa/s 8GHz Oscilloscope

5

- Apply calibration values with picosecond resolution
- Retain all of the accuracy gained in the calibration process

6

Disable scrambling to see the Start of Packet on the wire

7

Remove probe delays from measurements:

- Measure all cable delays and board delays using Time Domain Reflectometer (TDR)
- Minimize FPGA output delays on probe signals and compensate for speed of FPGA (Process Voltage Temperature)

8

1pps cable delays:

- Measure cable delays with TDR
- Cable delay can vary from 4.1ns/m to 5.2ns/m dependent on type of cable and the dielectric material used

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