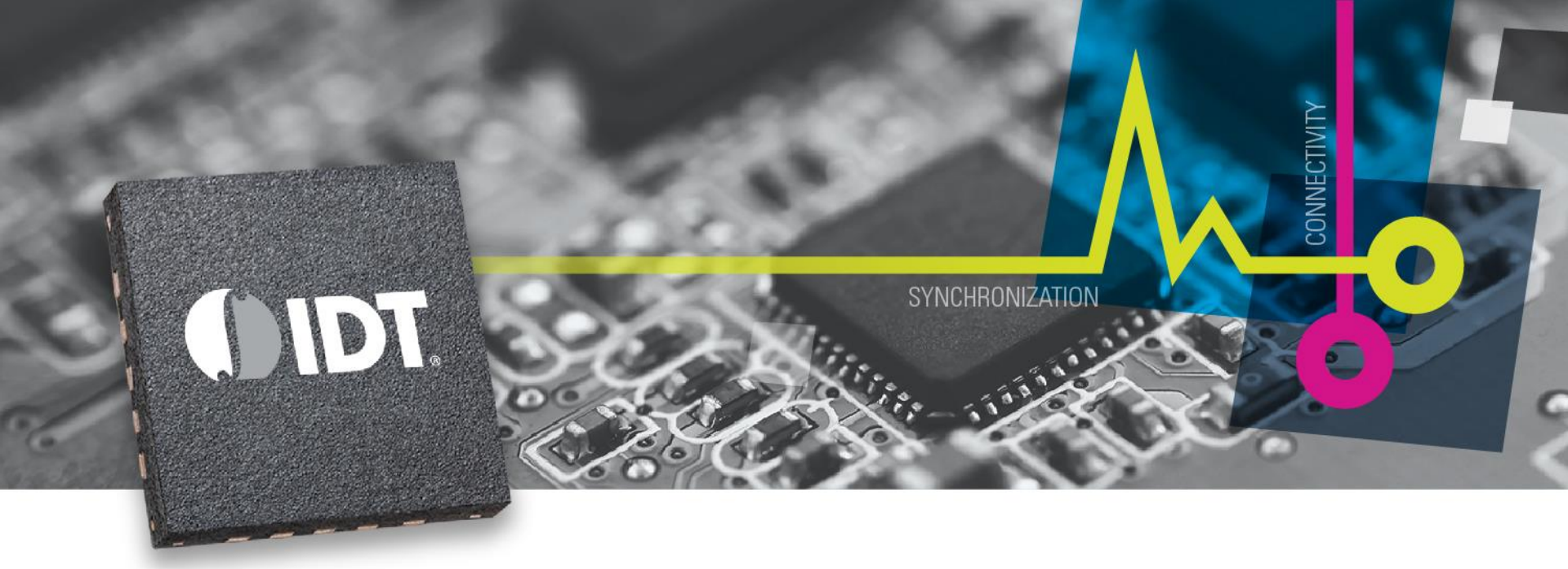


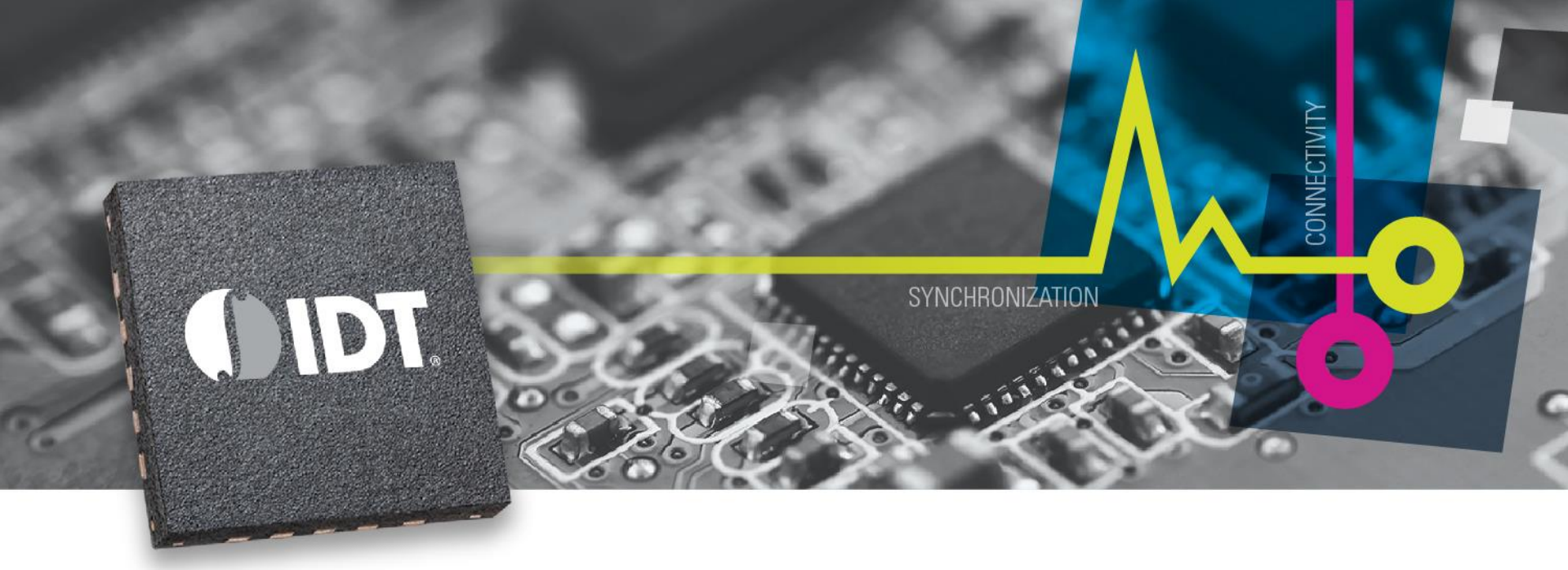
TUTORIAL: Phase Locked Loops

Greg Armstrong (Integrated Device Technology, Inc.)

March 18th, 2019

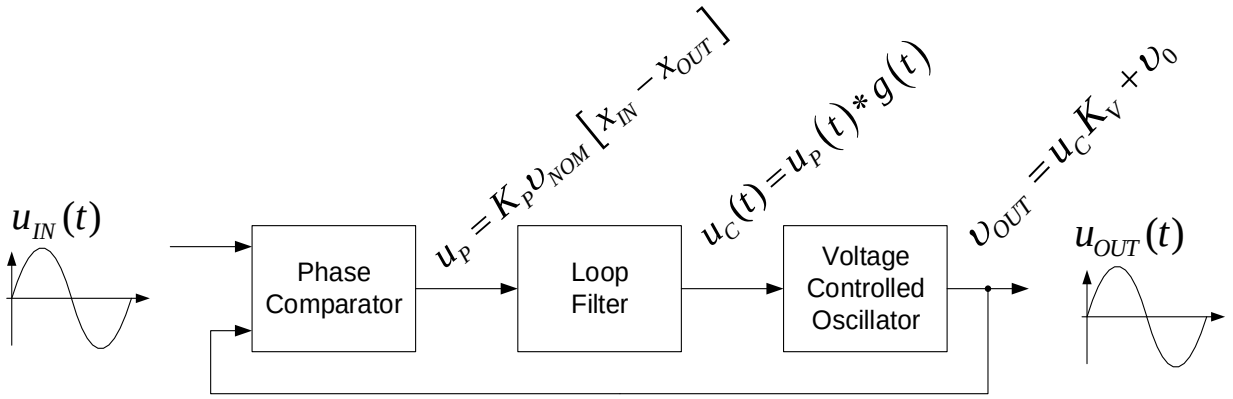
Outline

- Phase Locked Loops (PLL)
  - Principle
  - Response To Injected Noise
- PLL Operation Modes
  - Locked, holdover and freerun
- PLL with 2 inputs



Phase Locked Loops (PLL)

PLL: Working principle

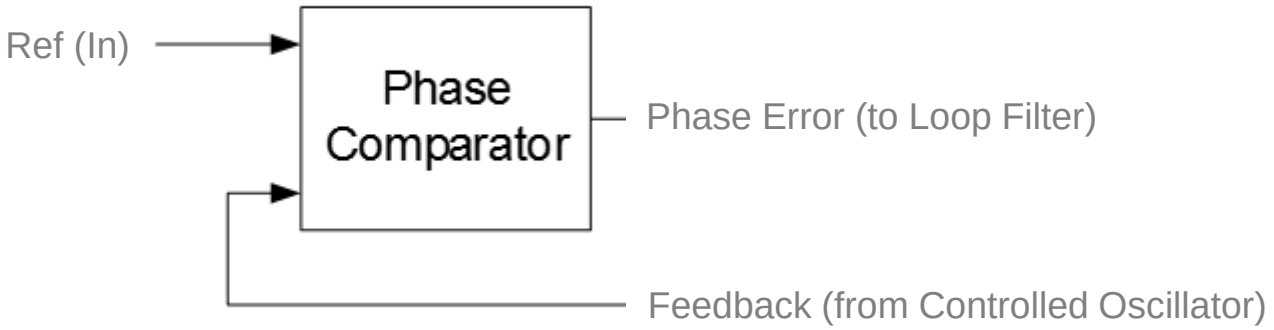


$$u_{IN}(t) = A \cdot \sin\left\{2\pi\upsilon_{NOM}\left[t + x_{IN}(t)\right]\right\} = A \cdot \sin\left\{2\pi\upsilon_{IN}(t) + \varphi_{0,IN}\right\}$$

$$u_{OUT}(t) = A \cdot \sin\left\{2\pi\upsilon_{NOM}\left[t + x_{OUT}(t)\right]\right\} = A \cdot \sin\left\{2\pi\upsilon_{OUT}(t) + \varphi_{0,OUT}\right\}$$

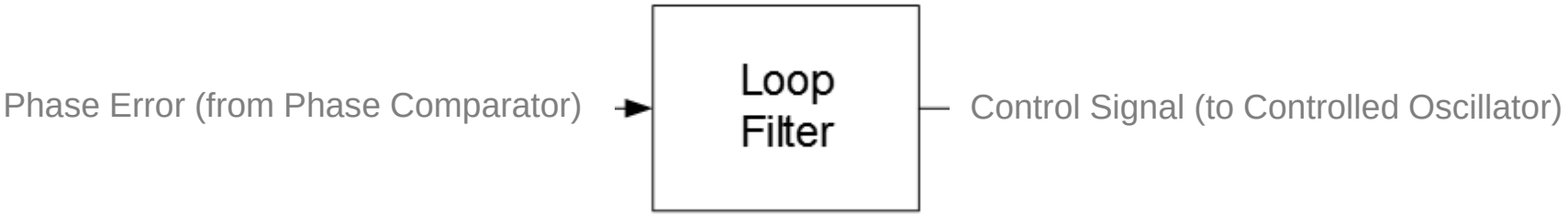
- A phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal
  - Bringing the output signal back to the input signal for comparison is called a feedback loop
- By keeping the input and output phase in lock, this implies that the input and output frequencies are the same as well
- PLLs generally generate an output frequency that is a multiple, or even a fractional multiple, of the input frequency
  - May requires an integer, or fractional, divider on the feedback
  - May require an integer, or fractional, divider on the input as well

PLL: Phase Comparator



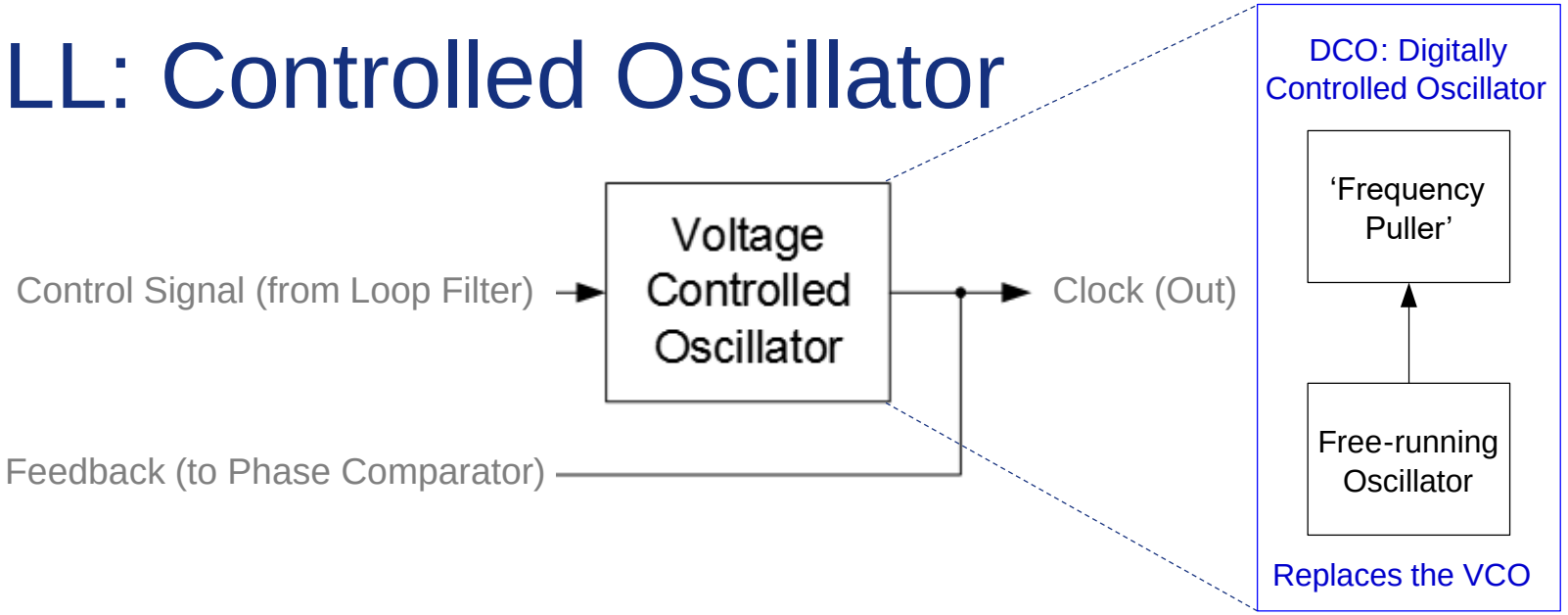
- The Phase Comparator establishes the “error” between the reference input and the clock output; using a feedback
- Most Digital PLLs (DPLLs) use a Time to Digital Converter (TDC) and Phase Frequency Detector (PFD) to measure the phase of the two clocks and produce a digital word representing the error
  - TDC can be looked at as a timestamper
- The TDC timestamps the reference and feedback edges, and the PFD mathematically tracks the phase offset between the selected reference and feedback clocks
- The measured phase difference can go well beyond 1 period, or Unit Interval (UI), of the reference and feedback clocks; thus, the phase comparator must be able to measure over a large range of multiple input/feedback clock periods
  - Various telecom standards define a jitter & wander tolerance requirement - the widest is defined is 18µspp
  - For example, if the input clock has a nominal period of 8ns (125 MHz), then the jitter tolerance requirement equates to ± 1125 UI

PLL: Loop Filter



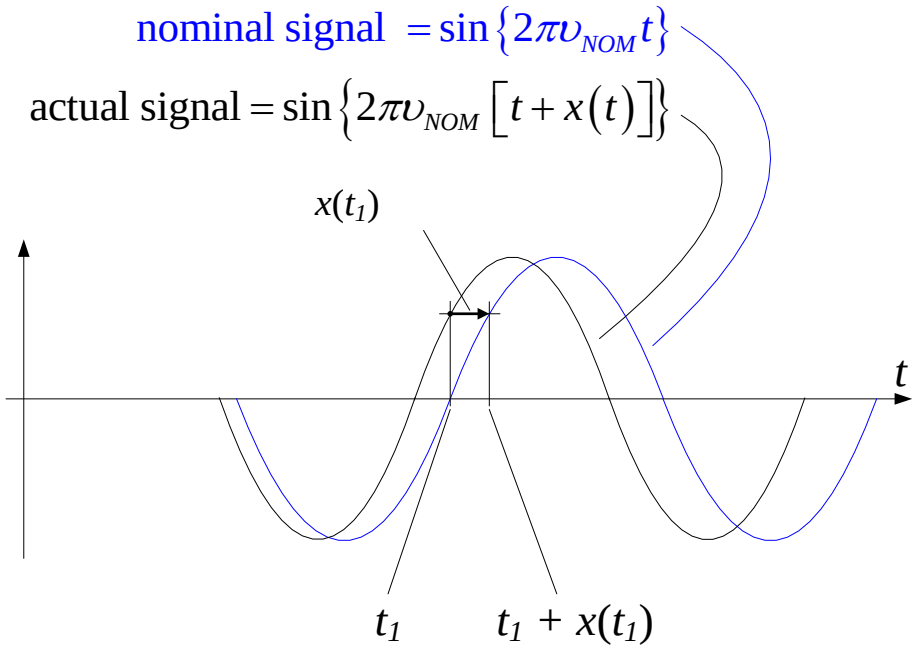
- The phase error is processed by the loop filter (LF)
  - LF is a combination of proportional and integral (PI) control, which generates a control signal for controlling the oscillator
- The LF determines the bandwidth (BW) of the PLL
  - Other functionality, such as phase slope limiting (PSL), locking range, and holdover functionality may be done as well
- Phase corrections mainly done through proportional path, along with any PSL
- Frequency offset, or drift corrections, is done through the integrator path, including damping (i.e. gain peaking control)

PLL: Controlled Oscillator



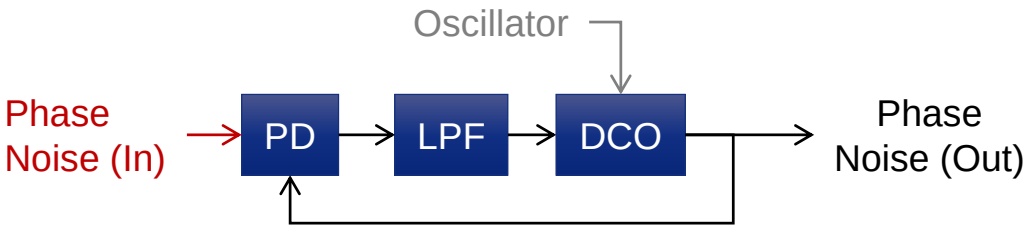
- The controlled oscillator uses the control signal to speed up or slow down the output clock
- Most Digital PLLs replace the Voltage Controlled Oscillator (VCO) by a Digitally Control Oscillator (DCO) consisting of:
  - a free-running crystal oscillator (XO)
  - A digital synthesizer which pulls the frequency up or down using a Control Signal from loop filter (a digital word representing a fractional frequency offset (FFO))

PLL: Phase-time deviation $x(t)$



Note: Phase-time x = random component only
Time Error TE = random and deterministic components

PLL: Response to Injected Noise



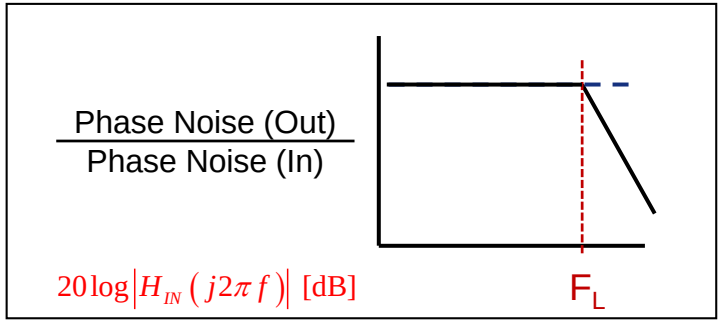
$$x_{OUT}(t) = x_{IN}(t) * h_{IN}(t)$$

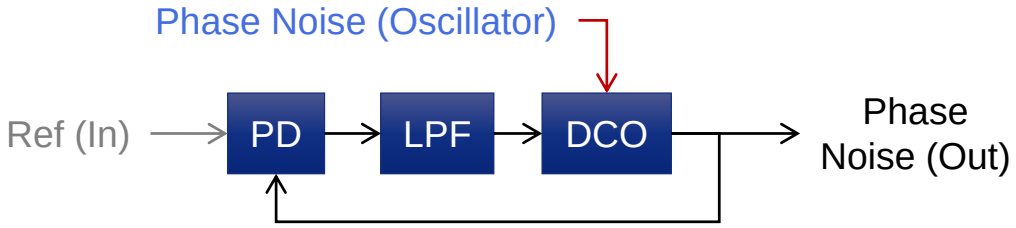
$$X_{OUT}(s) = X_{IN}(s) \cdot H_{IN}(s)$$

where $h_{IN}(t) =$ impulse response

$$H_{IN}(s) = \text{transfer function} = \text{Laplace}\{h_{IN}(t)\}$$

PLL is a low-pass filter for input noise





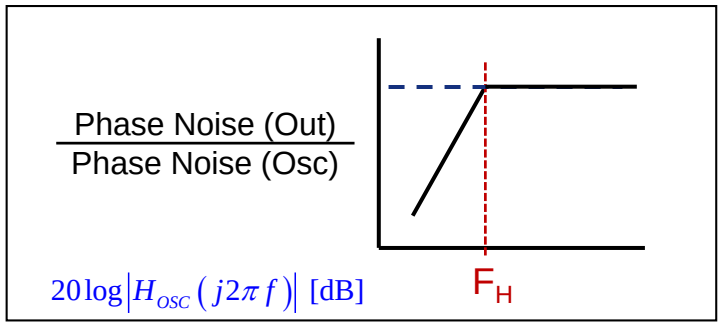
$$x_{OUT}(t) = x_{OSC}(t) * h_{OSC}(t)$$

$$X_{OUT}(s) = X_{OSC}(s) \cdot H_{OSC}(s)$$

where $h_{OSC}(t) =$ impulse response

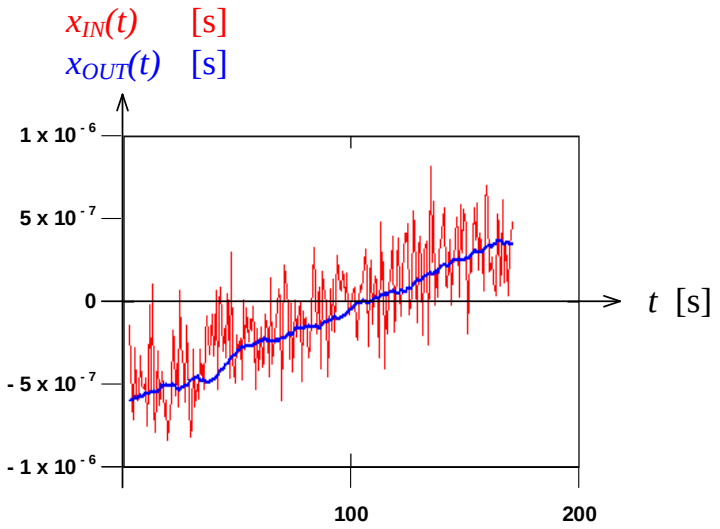
$$H_{OSC}(s) = \text{transfer function} = \text{Laplace}\{h_{OSC}(t)\}$$

PLL is a high-pass filter for oscillator noise

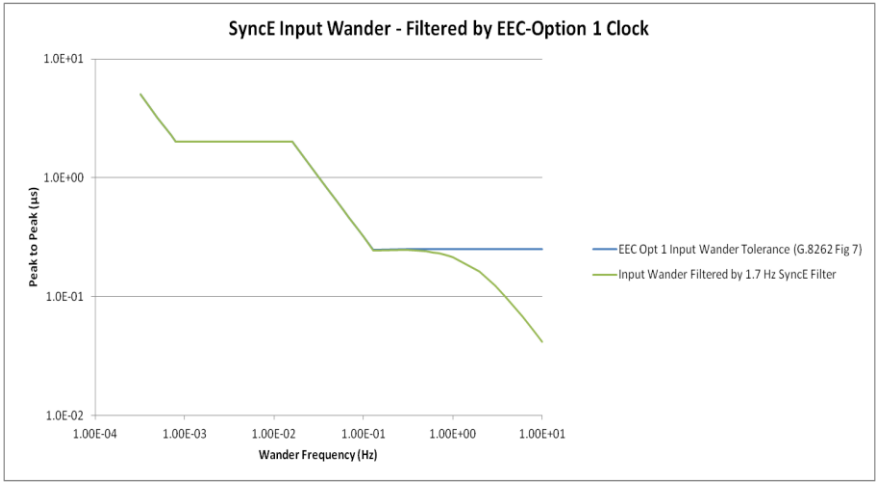


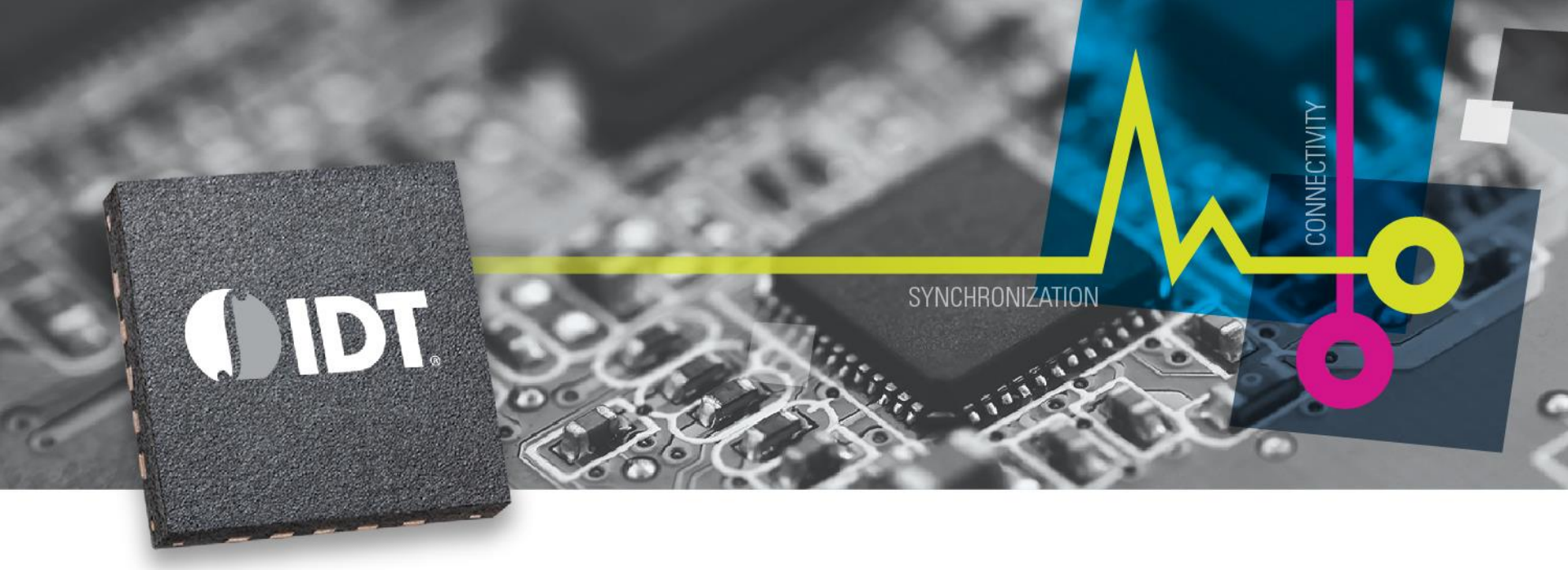
PLL: Jitter & Wander filtering

- What is jitter/wander?
  - Noise or other disturbances on the clock when compared to an ideal reference
    - Jitter = short-term variations
    - Wander = long-term variations
  - ITU-T G.810 defines noise frequencies <10Hz as wander and frequencies ≥10Hz as jitter



- The function of a PLL is to attenuate jitter and transfer wander
  - In other words, tolerate noise at the input without losing lock to the reference





PLL Operation Modes

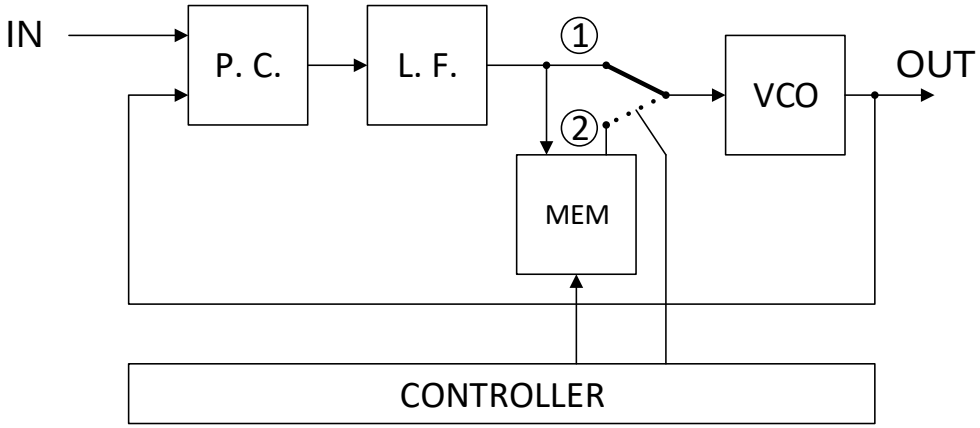
PLL Modes: Locked, holdover and freerun

- Locked mode: clock has a valid input signal, PLL loop is closed, i.e. switch is in position 1.
- Freerun & holdover modes: no valid input signal is detected, controller switches to position 2, clock becomes an autonomous synchronization source.

Holdover: memory MEM remembers last locked mode frequency

Freerun: value in the holdover memory is invalid or outdated

After entry into freerun or holdover mode, frequency is subject to ageing drift and to the influence of temperature.



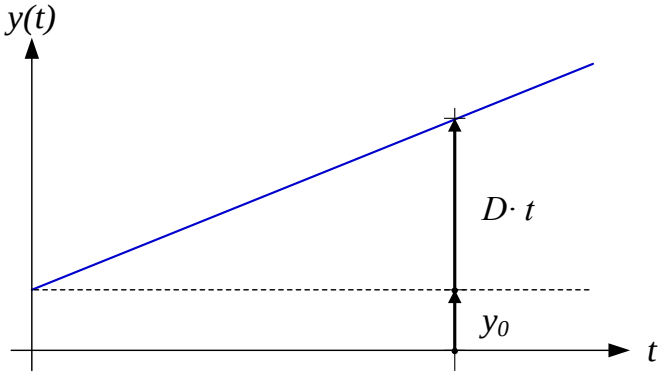
PLL Modes: Holdover @ constant temperature

Fractional frequency:

$y(t) = y_0 + D \cdot t$

where $y_0 =$ initial frequency offset

$D =$ frequency drift rate (constant)



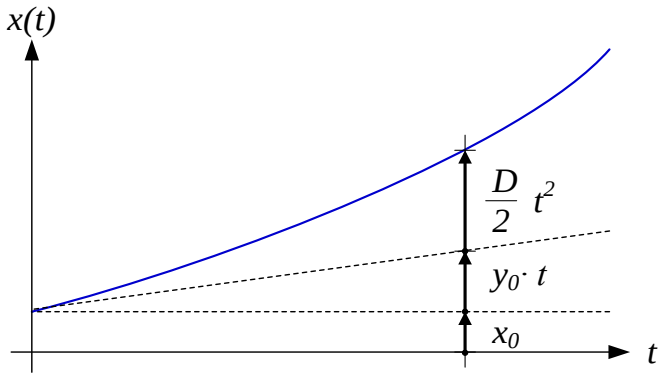
Time error:

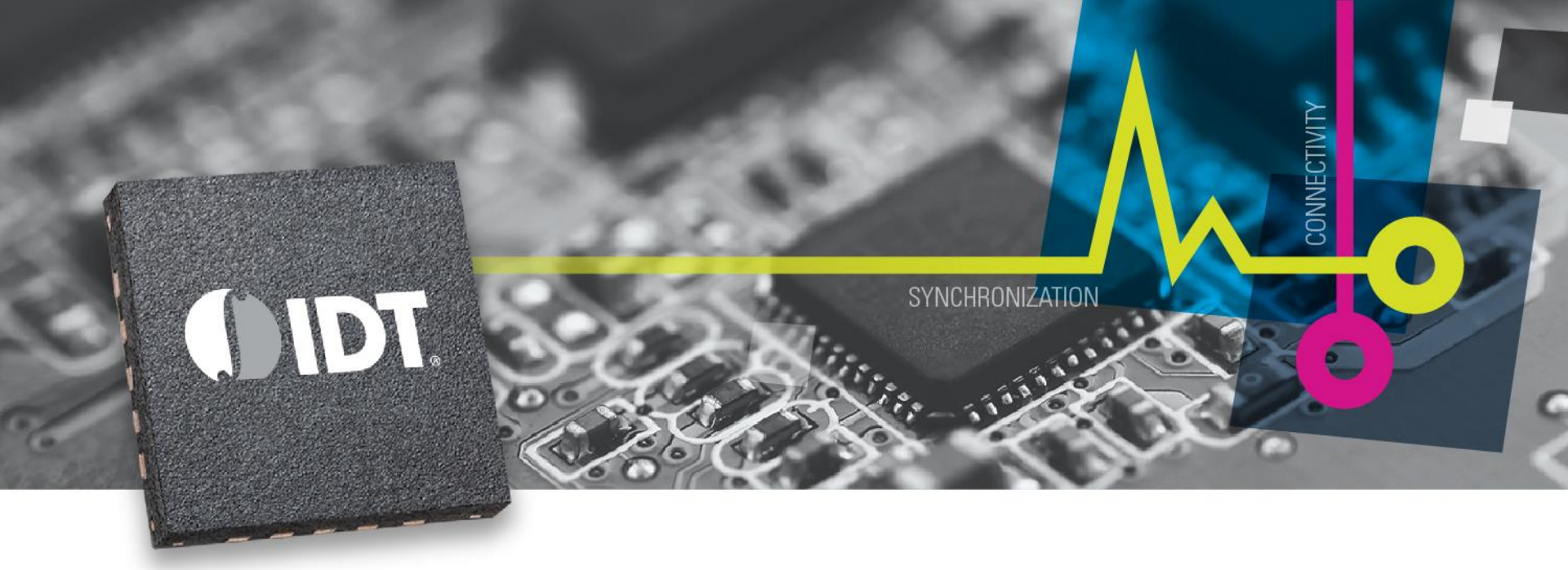
$$x(t) = x_0 + y_0 \cdot t + \frac{D}{2} \cdot t^2$$

where $x_0 =$ initial phase offset

$y_0 =$ initial frequency offset

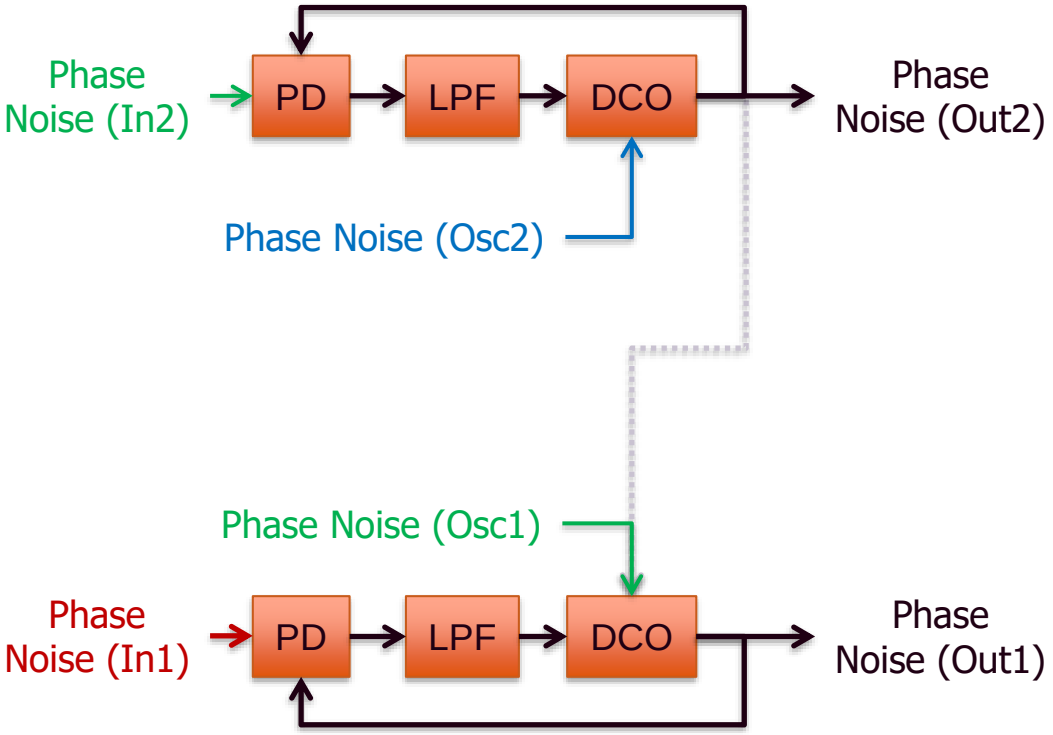
$D =$ frequency drift rate (constant)

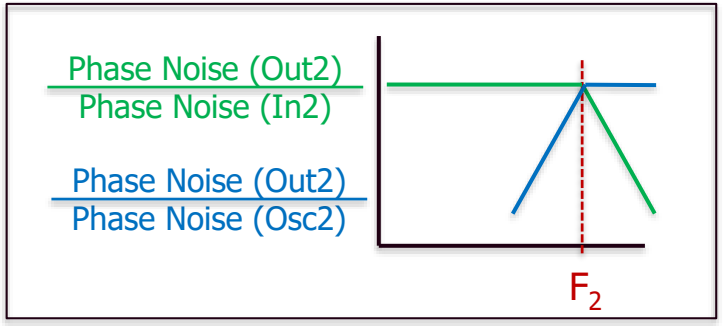


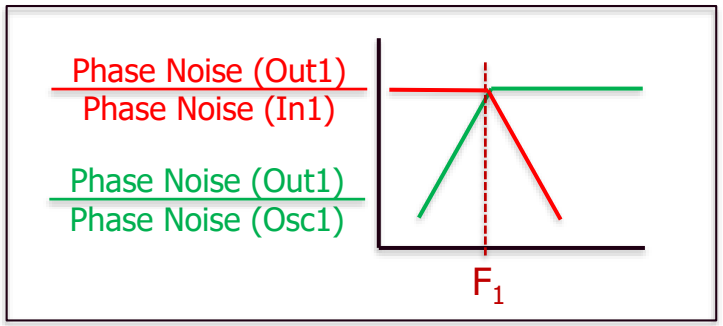


PLL with 2 Inputs

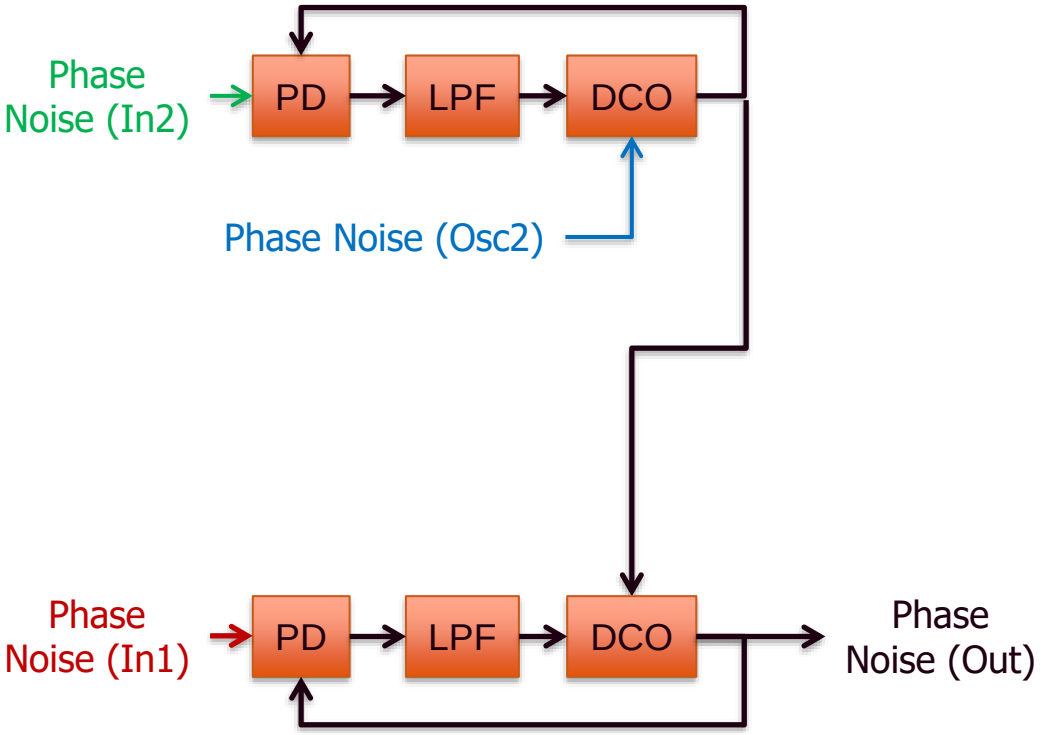
Combining two PLLs



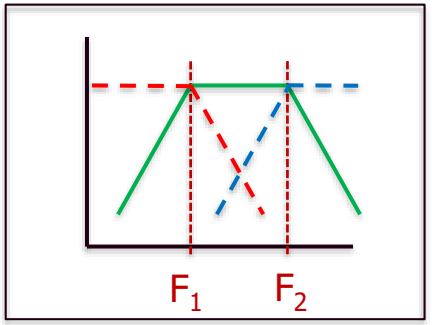




Two PLLs: Response to Injected Noise

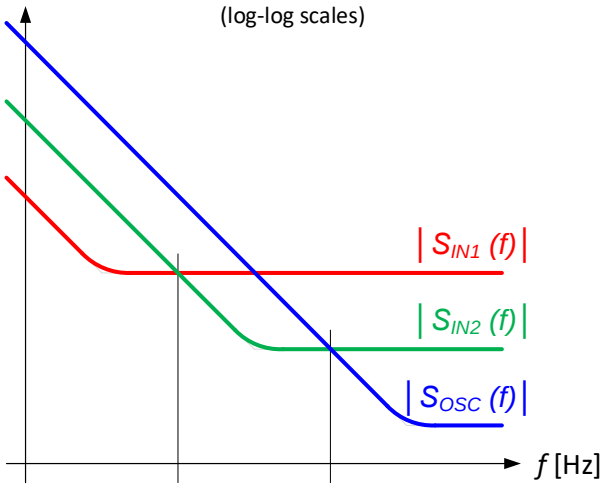


Band-pass filter for In2 Noise to Out

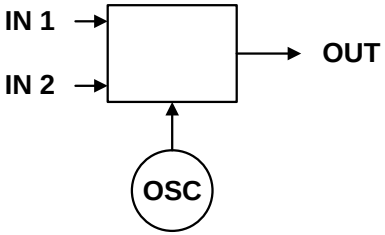


Two PLLs: Spectral densities

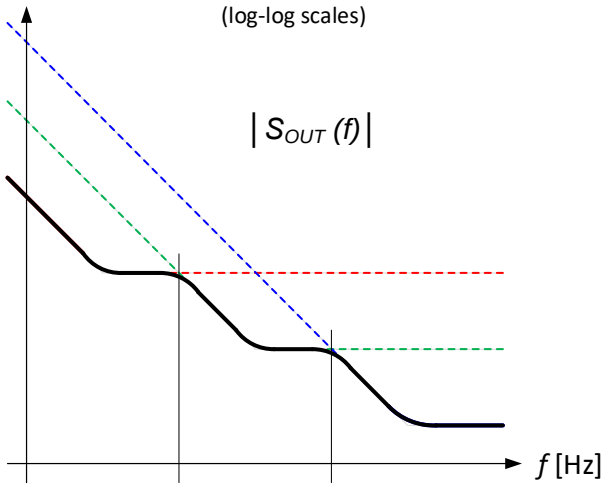
Three spectral densities (phase-time) …



… combined by the 2-input PLL, …

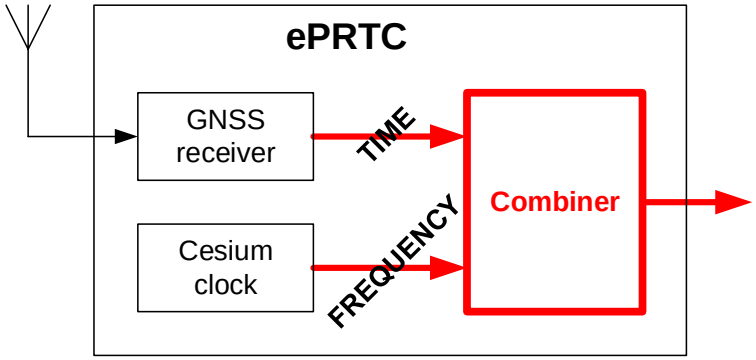


… result in this out spectral density:

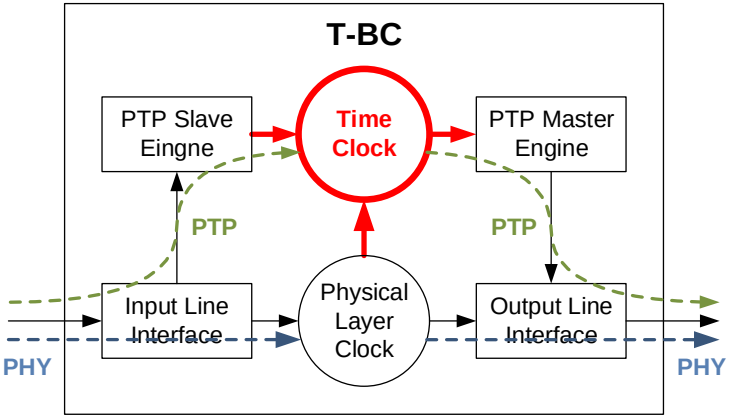


Two PLLs: Applications

- **GNSS & Cesium clock** in enhanced Primary Reference Time Clocks (ePRTC)

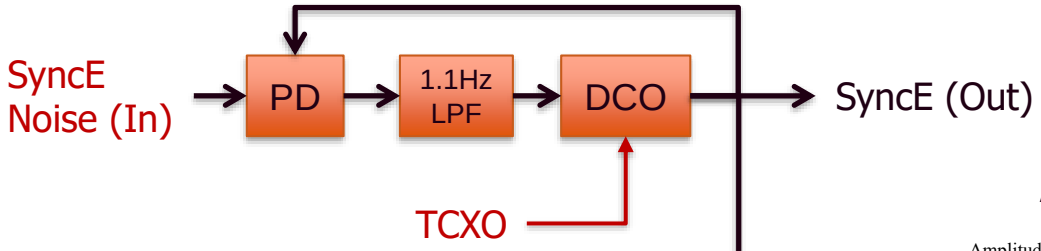


- **PTP & SyncE** in boundary clocks (T-BC) and slave clocks (T-TSC)

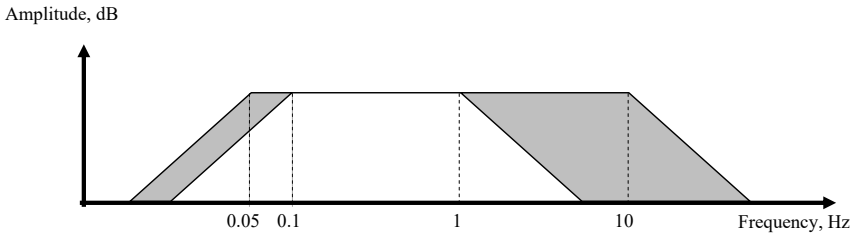


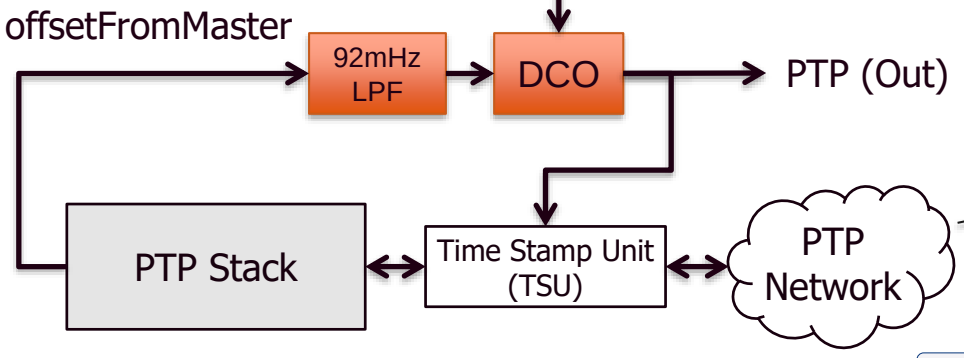
- Note: PLL with 2 inputs is not the only way of combining 2 references

T-BC: Response to Injected SyncE Noise

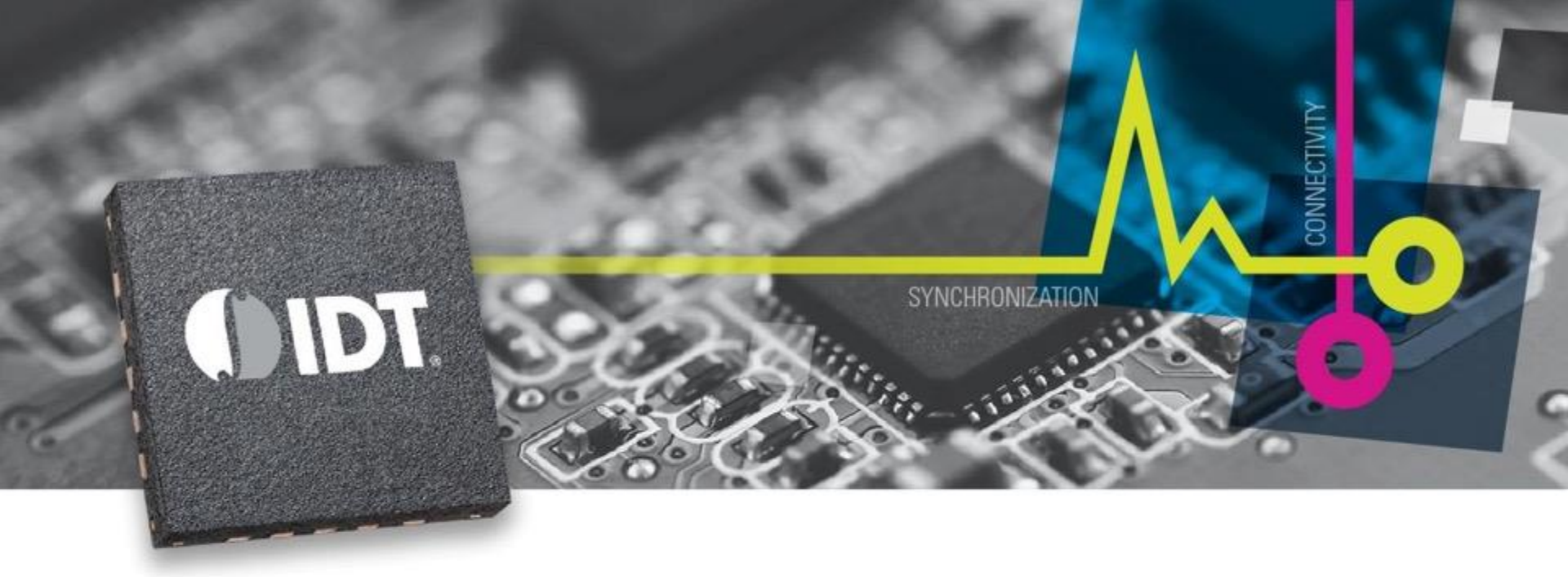


A band-pass filter for SyncE Noise to PTP (Out)





Very little PDV



Thank You

Analog Mixed Signal Product Leadership in Growth Markets