Clock Classification for Time & Phase Synchronization Applications

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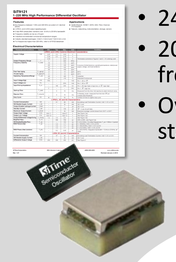
Today's dilemma: Disconnect between clock spec & system requirements

What you get from Stratum clocks



- 24-hr frequency holdover
- 20-year free running frequency accuracy
- Over-temp frequency stability

What matters to time sync systems

- Holdover in time
- ADEV, ΔF/ΔT, short-term drift
- Environmental factors (temp profile, vibration, airflow)

Stratum 3 or Stratum 3E or Stratum 2?
Actual holdover under real operating conditions?
Stratum level frequency holdover = time/phase holdover?
Over-paying OCXO for clock recovery?

INTRODUCTION

Stratum levels are commonly used for specifying clock requirements for frequency synchronization systems. This scheme does not provide relevant performance metrics for phase and time synchronization applications that rely on packet based synchronization protocols such as IEEE 1588. Clock standardization based on phase stability would close the gap between component specifications and system requirements in time sync.

"Phase stability" based clock standards: Connect spec to system needs

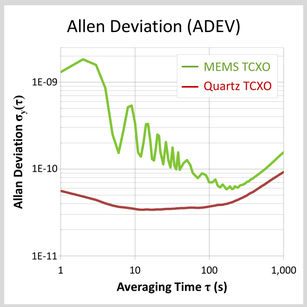
Clock standards by Industry Standards Group

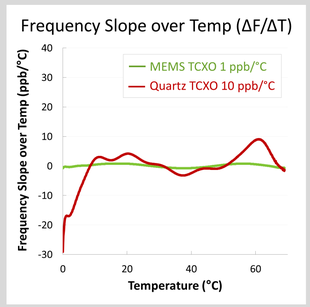
- Specify phase sync related clock requirements - ΔF/ΔT, ADEV, short term aging
- Identify environment factors (airflow, vibration)
- Provide models to correlate between clock spec to system performance

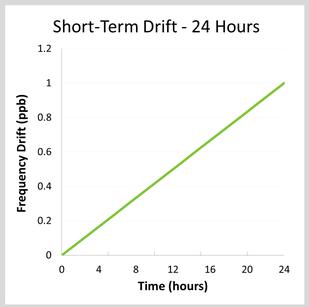
Certification Eco-system

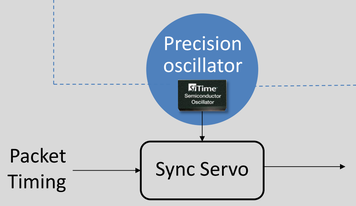
- Certification by trusted third party test labs
- Benchmarking using consistent methodologies
- Performance data for clock selection

Clock specs that impact time/phase accuracy







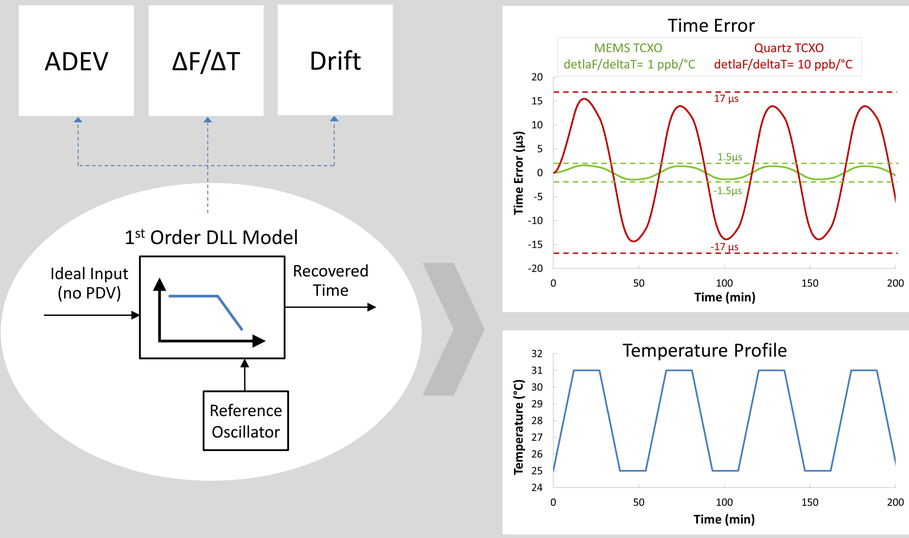


BACKGROUND

Allen deviation (ADEV), short-term drift and ΔF/ΔT are critical to a given time and phase synchronization capability. Environmental stressor such as airflow can also significantly impact synchronization accuracy.

A delay locked-loop (DLL) first order response model connects clock performance to system time error under different operating profiles.

Connect clock specs to system time error with DLL model



Phase stability levels and environmental grades

Phase Stability | Operating Grade

PhT XXXX Y - ABC

Phase/ Time	Time Accuracy	Time Constant/ Holdover	TempRamp	Vibration	Airflow
	- 100 nsec - 500 nsec - 1500 nsec - 5000 nsec	- A = 24 hrs - B = 8 hrs - C = 4 hrs - D = 30 min - E = 10 min - F = 1 min	- A - B - C - D	- A - B - C - D	- A - B - C - D

Operating grades can be benchmarked based on the operating profiles defined in the proposed standards

PROPOSAL & BENEFITS

This new classification proposal defines clock performance in terms of time and phase errors and holdover capabilities under real life conditions.

The key objective is to enable engineers to efficiently specify the most optimal clock requirements for a given system sync accuracy. This clock standardization model will provide benefits at all levels, from suppliers to equipment makers and operators.

Everyone benefits from clock standardization

OPERATORS
Peace of mind
Objective system evaluation

CLOCK SUPPLIERS
Performance differentiation
Value based pricing

EQUIPMENT OEM/ODM
Simpler clock selection
No over-spec/over-spending

ACADEMIC/INDUSTRY LABS
$$$ from testing service
Research sponsorships