

Proving Performance of Packet Sync Equipment and Networks

Tommy Cook,
CEO


Calnex



www.calnexsol.com

Presentation overview

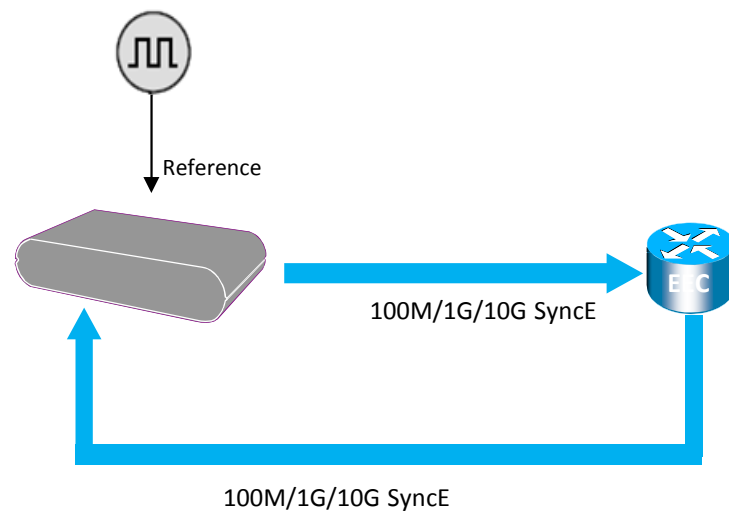


Proving performance of;

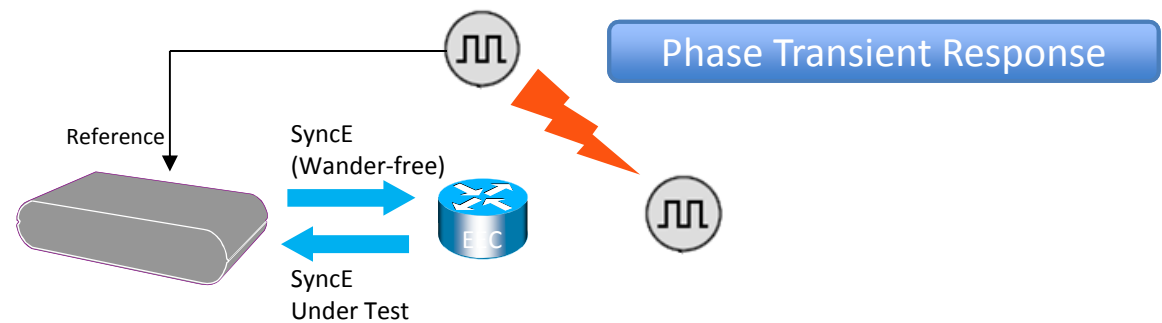
- **EEC - Synchronous Ethernet Devices.**
- **1588v2 Devices.**
 - **Measurement Plane concept.**
 - **Boundary Clocks.**
 - **Transparent Clocks.**
 - **Ordinary Clocks.**
- **Networks**
 - **Packet Network Metrics**
 - **Proof of Concept trials (experimental results)**

EEC – Synchronous Ethernet devices

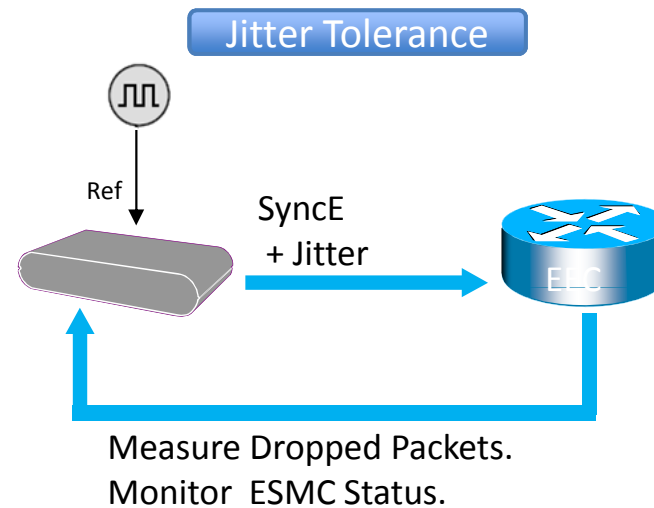
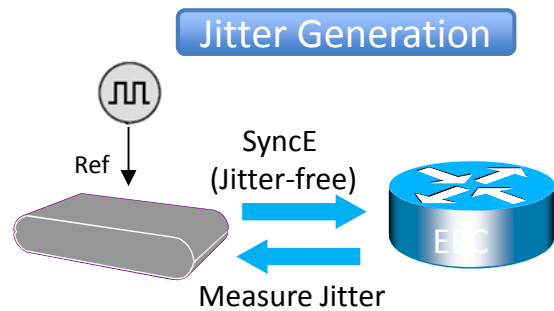
Sync-E Wander to G.8262



- Frequency Accuracy
- Pull-in, Pull-out, Hold-in
- Wander Generation
- Wander Tolerance
- Wander Transfer



Sync-E Jitter to ITU-T G.8262



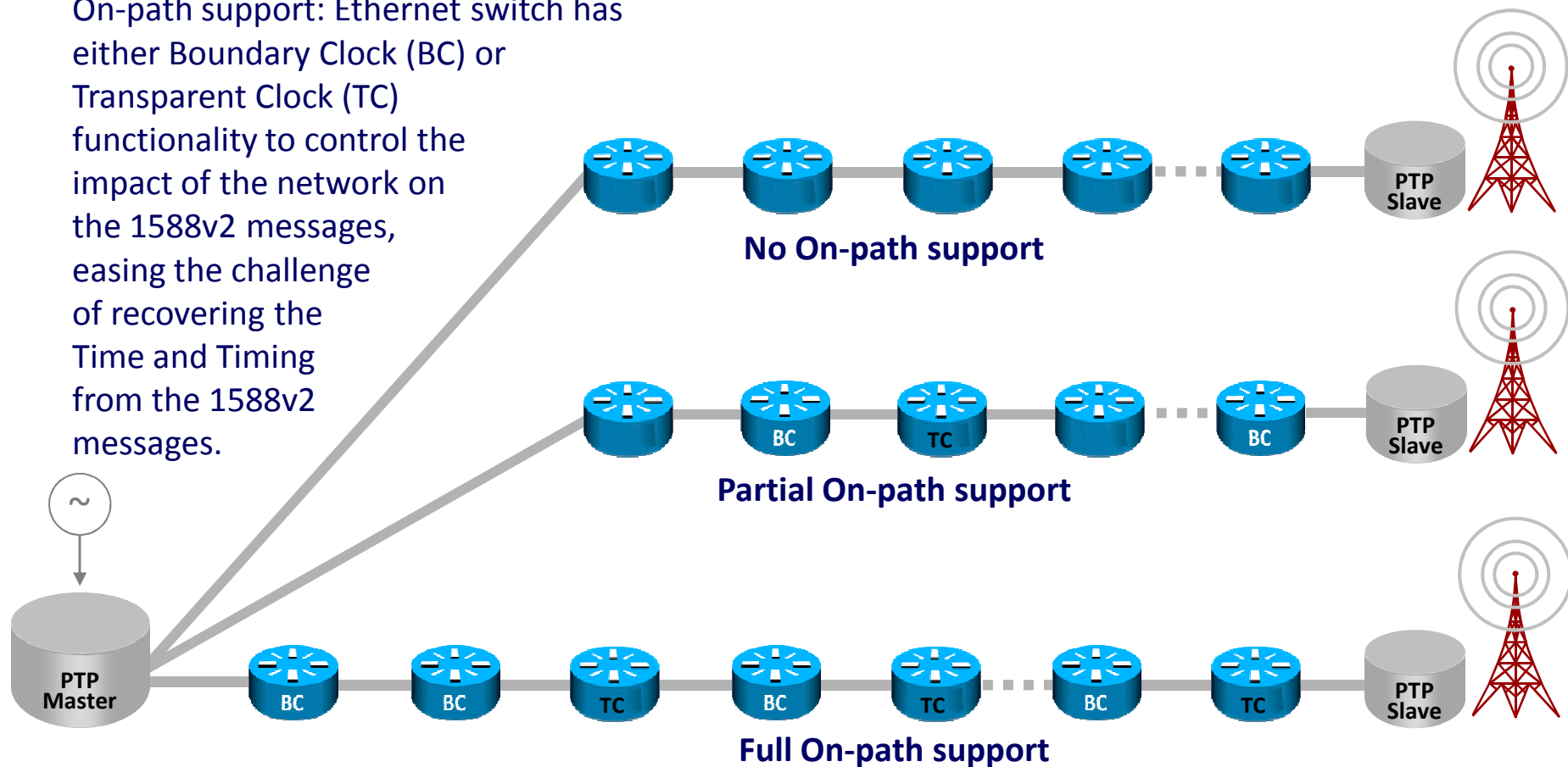
- No dropped packets indicating bit errors being introduced.
- Not causing any alarms.
- Not causing the clock to switch reference.

1588v2 Devices

Designing your network



On-path support: Ethernet switch has either Boundary Clock (BC) or Transparent Clock (TC) functionality to control the impact of the network on the 1588v2 messages, easing the challenge of recovering the Time and Timing from the 1588v2 messages.



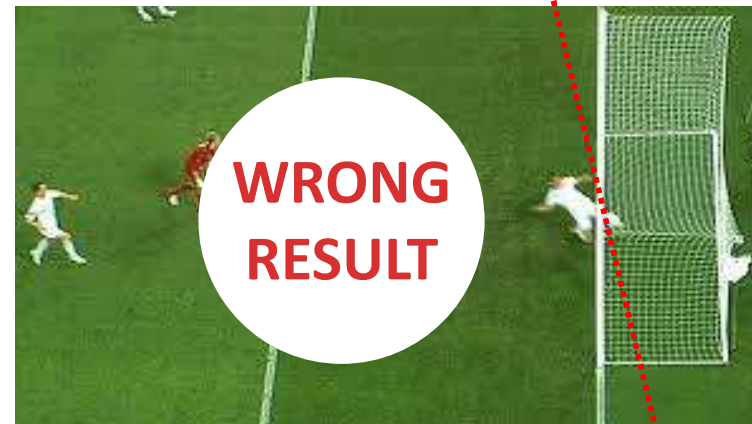
Measurement Plane concept

Measurement plane alignment ... GLT analogy



In 2012, the European Championship co-hosts Ukraine were denied an equaliser in a decisive 1-0 defeat to England when officials failed to spot Marco Devic's shot had crossed the line.

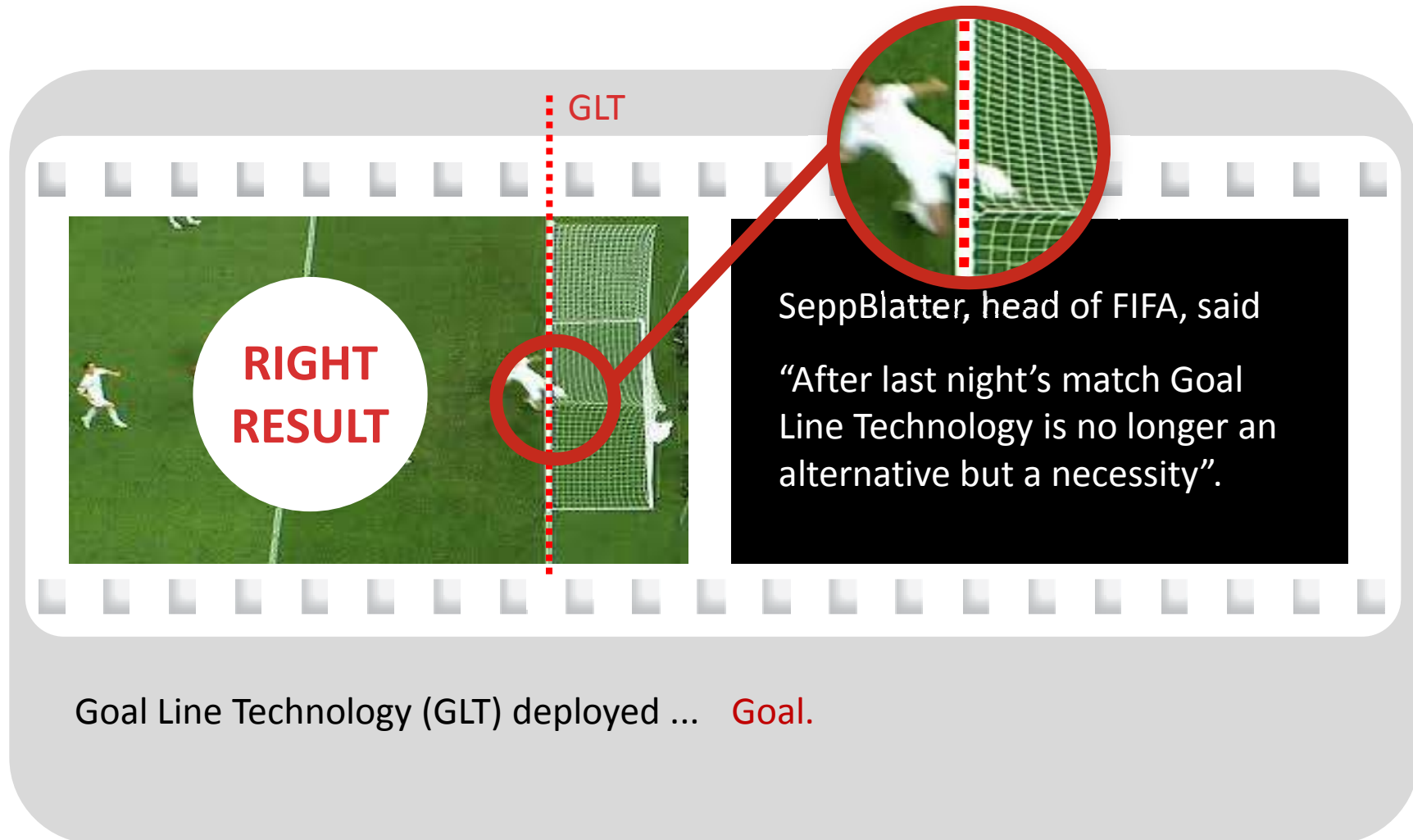
Measurement plane alignment ... GLT analogy



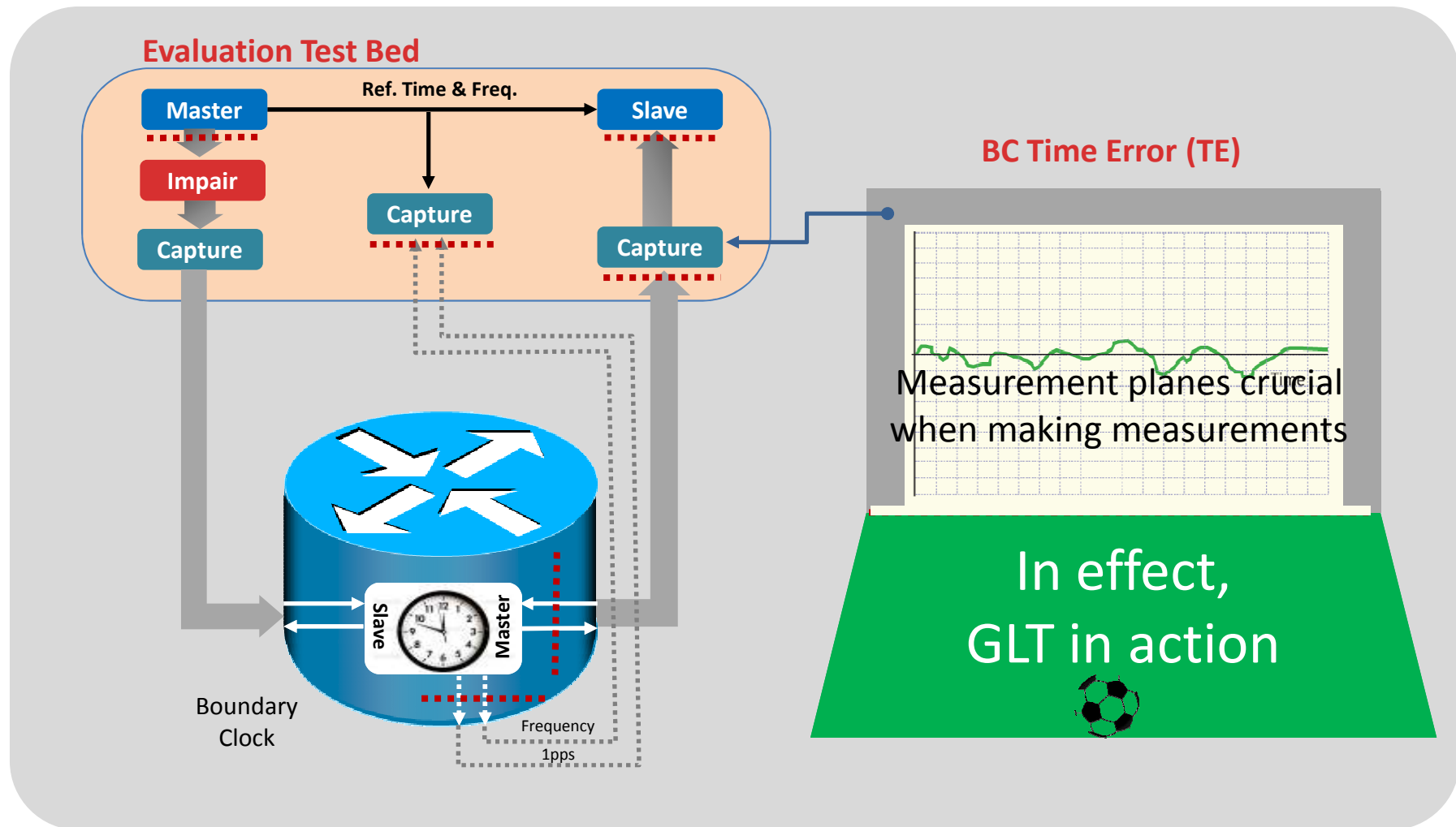
The Official's view?

Uncertainty, therefore no goal.

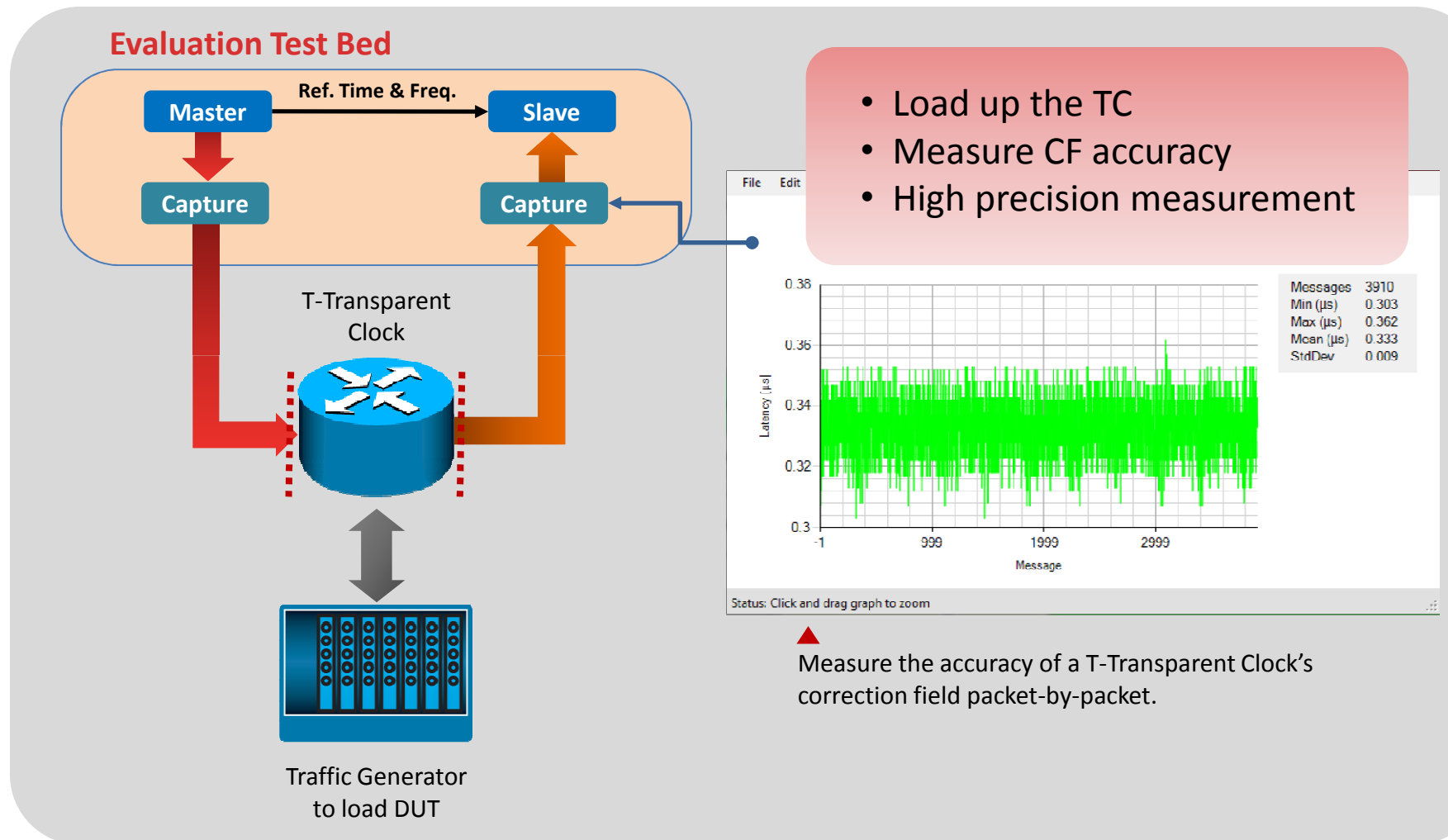
Measurement plane alignment ... GLT analogy



Boundary Clock testing: Measurement Plane

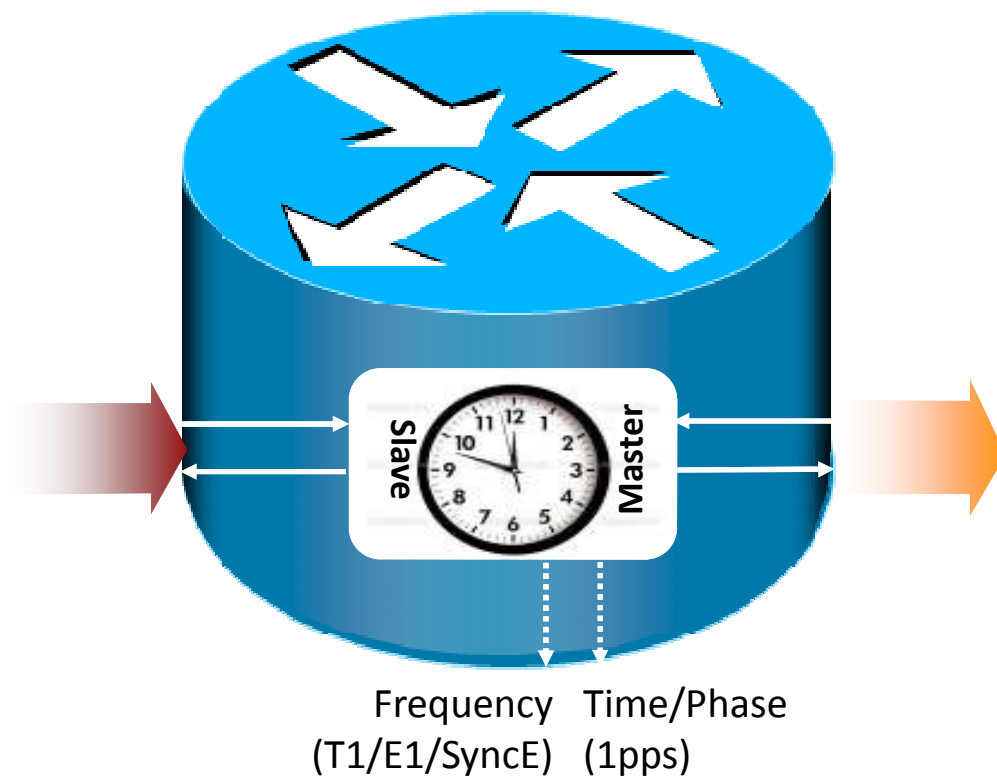


Transparent Clock testing: Measurement Plane



Boundary Clocks

Boundary Clock



Boundary Clocks reduce PDV accumulation by;

- Terminates the PTP flow and recovers the reference timing.
- Generate a new PTP flow using the local time reference, (which is locked to the recovered time).
- No direct transfer of PDV from input to output.

Boundary Clock is in effect a back-to-back Slave+Master.

Performance specification of a T-BC



Draft ITU-T **G.8273.2** will specify the performance of a BC. A number of sections have been proposed;

6. Physical Layer Performance requirements (G.8262 when SyncE supported)

7. Packet layer performance requirements

7.1 Noise Generation

7.1.1 Constant time error generation

7.1.2 Time noise generation

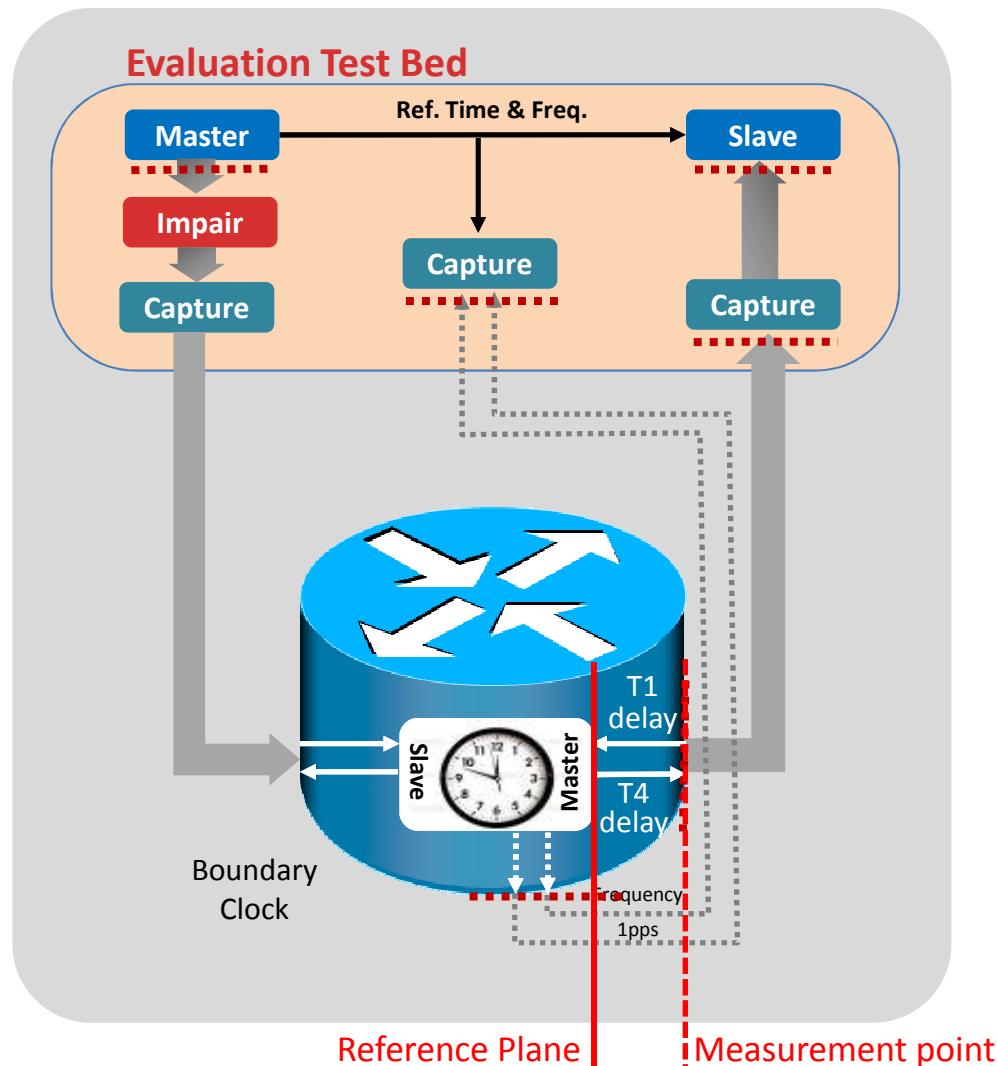
7.2 Time Noise Tolerance

7.3 Time Noise Transfer

7.4 Packet Layer Transient and Holdover Response

The structure in G.8273.2 is following the well established methods of specifying the performance of node clocks (e.g. in G.8262 for SyncE, etc.) but with the additions particular to the transfer of Time.

T-BC Time Error



TE: Difference between recovered time in the T-BC to the Master's Time.

- **Max TE** (absolute wrt ref)
- **Dynamic TE, MTIE/TDEV**
- **Constant TE** (absolute wrt ref)

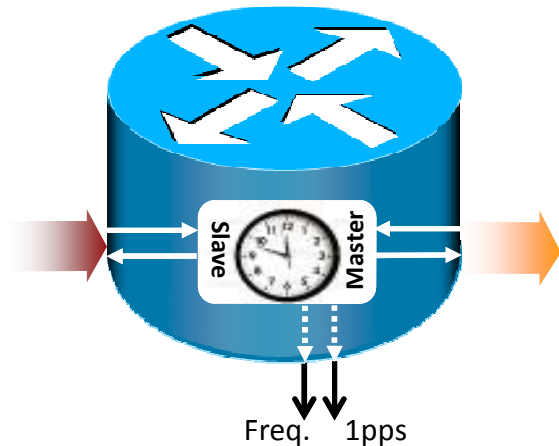
a) Measure 1pps;

- If 1pps available, compare to 1pps from Master reference to determine accuracy.

b) Measure Egress 1588v2;

- Analysis timestamps to determine TE of T-BC.
- Need to include t1 and t4 delays to measure Time output as seen by downstream device.

T-BC test results example



Devices that utilise SyncE, it is important to verify;

- SyncE performance to G.8262.
- Time transfer performance to G.8273.2, (under dev.).
 - As well as tolerance to 1588v2 noise, check Time performance when exposed to SyncE physical layer noise.

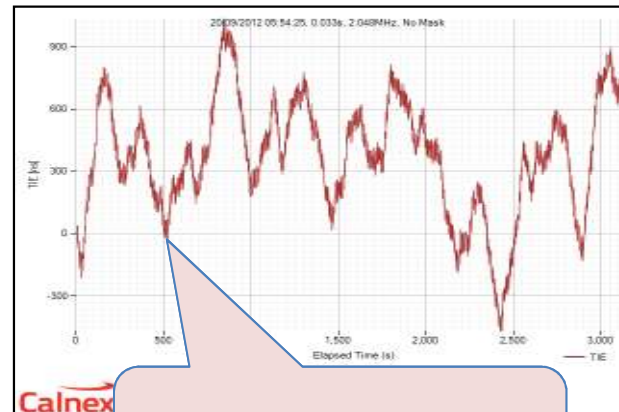
Stimulus;

- TDEV SyncE noise injected to ingress port.

Measurement;

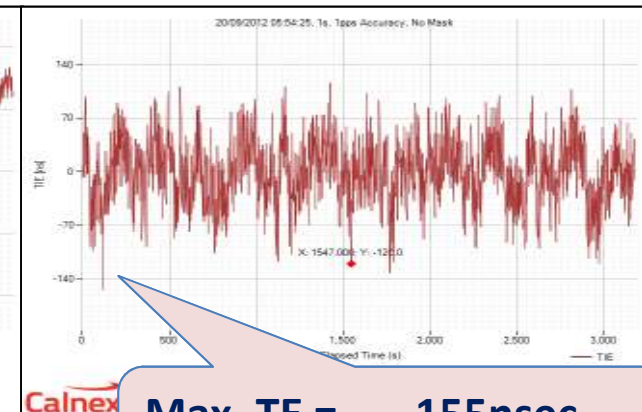
- Frequency Response
- Time Response

Freq. Response,
2M Clock output



810nsec pk-to-pk

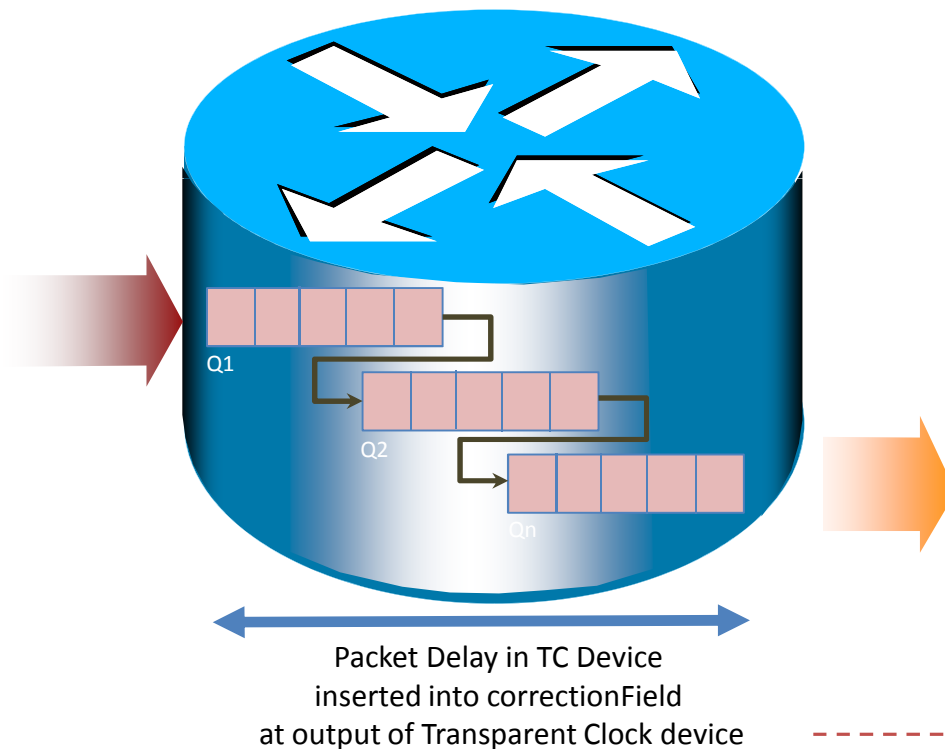
Time Response,
1pps output



Max. TE = 155nsec
Constant TE = 14nsec

Transparent Clocks

Transparent Clock



Transparent Clocks reduce PDV by;

- Calculating the time a PTP packet resides in the TC device (in nsec) and insert the value into the correctionField.
- By using the correctionField, the Slave or terminating BC can effectively remove the PDV introduced by the TC.

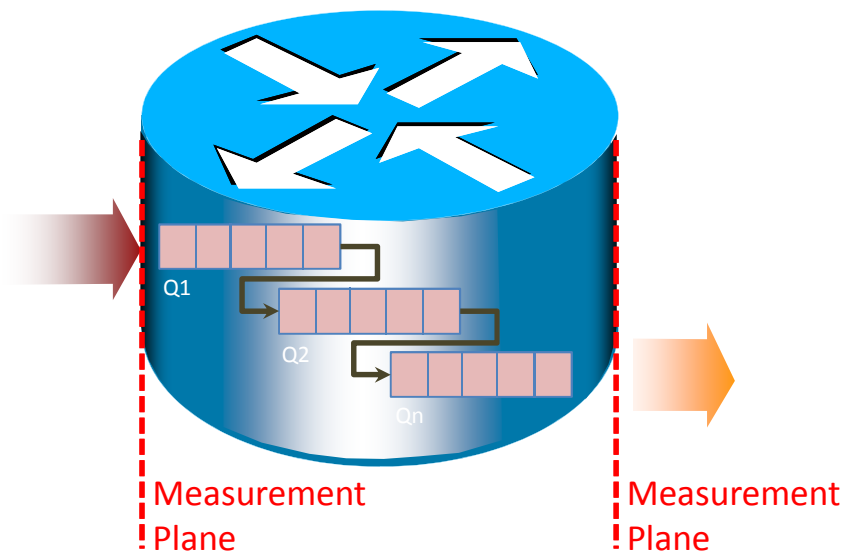
PTP Message Header Format							
Bits							
7	6	5	4	3	2	1	0
transportSpecific				messageType			
Reserved				versionPTP			
messageLength							
domainNumber							
Reserved							
Flags							
----->				correctionField			
Reserved							

Accuracy of the CorrectionField value:

Does it reflect the actual delay experienced by the Sync & Del_Req messages?

Theoretical model:

- CorrectionField precisely reflects the delay through the equipment
- Ideal case – **zero net PDV**



Types of CorrectionField inaccuracy;

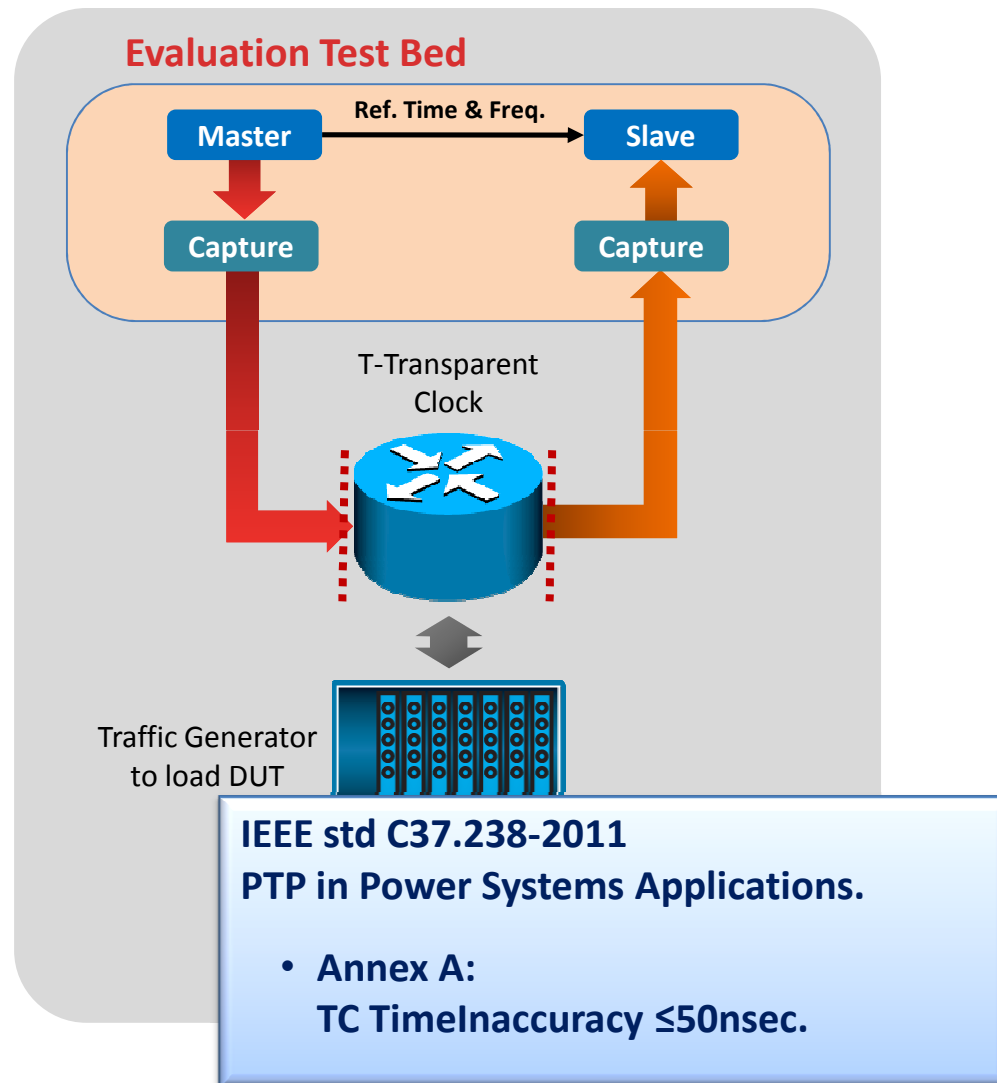
1. Variable error

- Caused by packet-to-packet variation in CorrectionField accuracy.
- **Leads to residual PDV when PTP terminated.**

2. Fixed Error

- Caused by CorrectionField value always being greater than a fixed value.
- Results in a fixed delay being measured when PTP terminated.
- **Not as issue if Fixed Error is matched in forward and reverse direction.**
- **Differences between forward and reverse Fixed Error will produce asymmetry and hence create a fixed Time Error.**

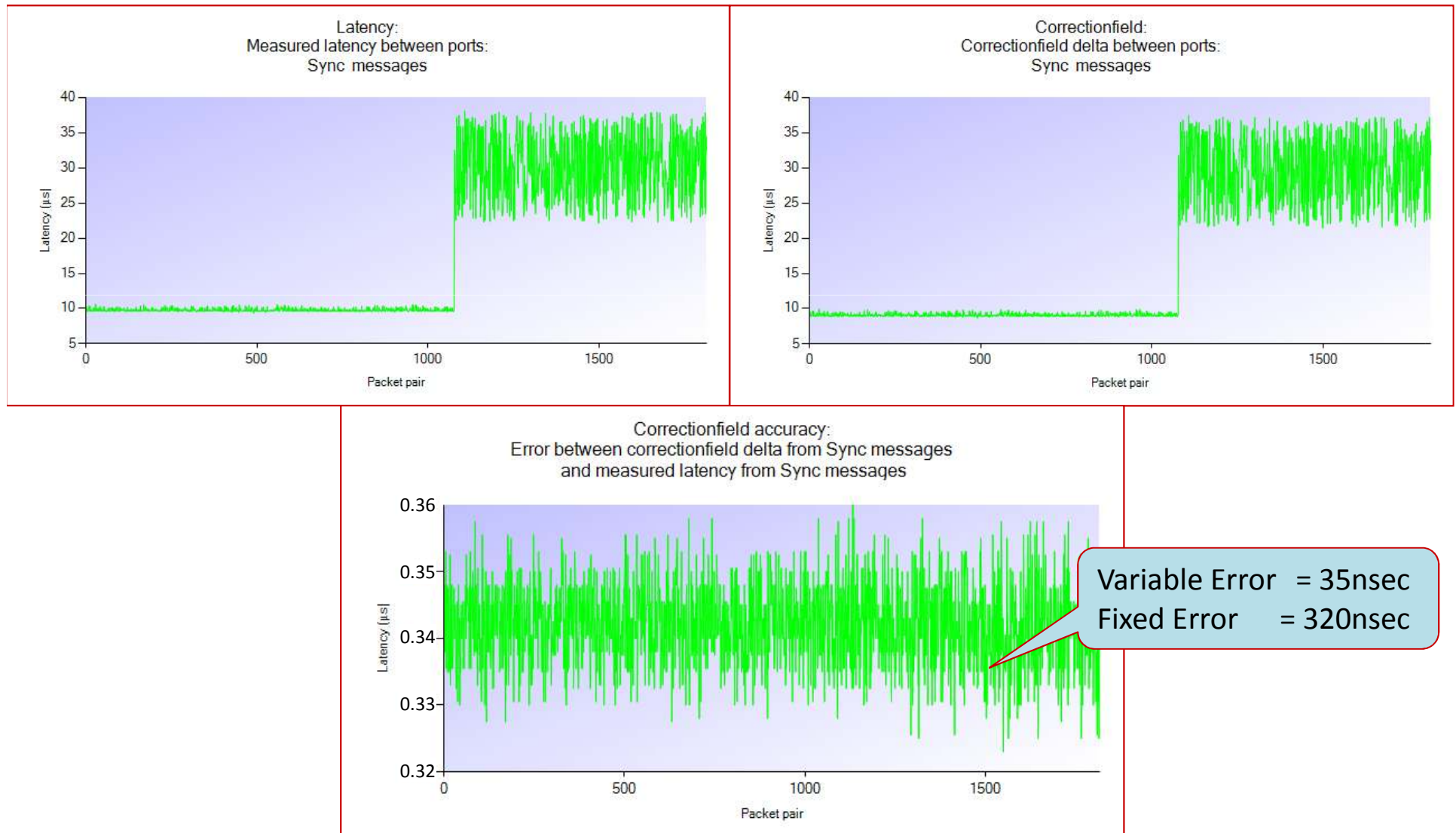
Transparent Clock Test Plan



Development Test Procedure to characterise actual performance

1. Measure the packet-by-packet latency across the TC.
 2. Determine the change to the correctionField value for each message.
 3. Accuracy is the difference in the actual latency compared to the change in Correctionfield value.
- Measure impact of CorrectionField on Sync PDV.
 1. Vary traffic packet size.
 2. Vary traffic priority.
 3. Vary traffic utilisation.
 - Repeat for Sync & Del_req PDV. Test in 1-Step and 2-Step modes.

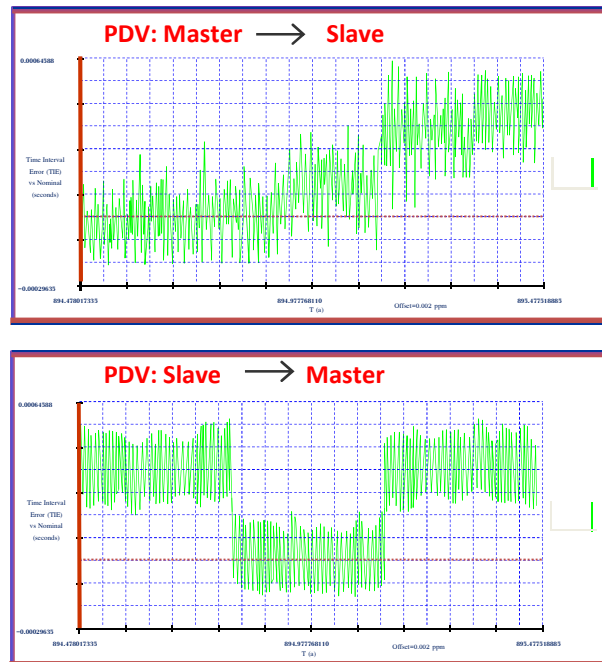
TC CorrectionField Accuracy example results



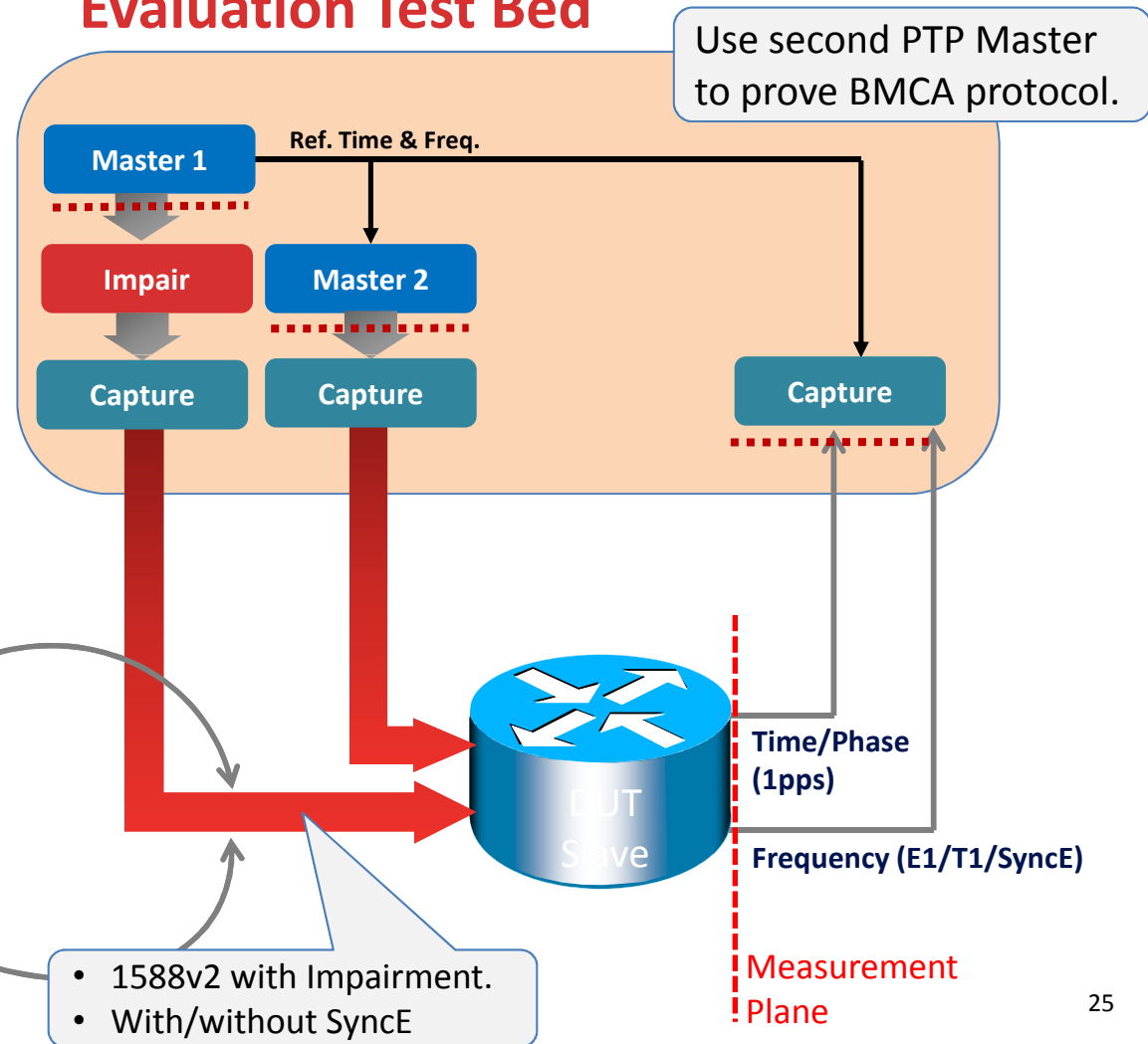
Ordinary Clocks

Prove performance of Slave Device

- Congestion in both directions will impact clock recovery.
- **G.8261 Appendix VI** Test Cases are the most widely used approach to verifying operation.



Evaluation Test Bed





Networks

PDV Metrics

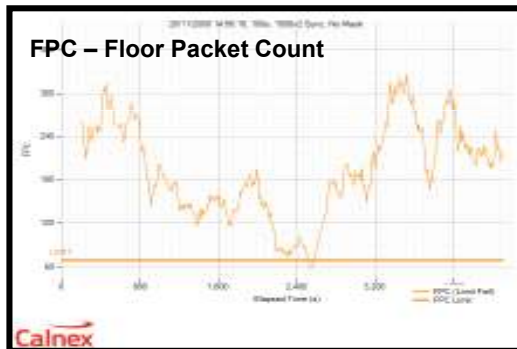
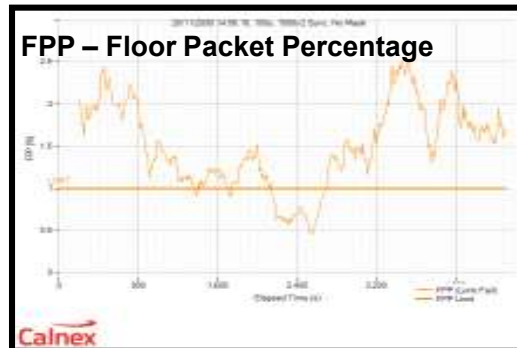


ITU-T G.8260: Appendix I defines a number of metrics that may be used for analysis of PDV.

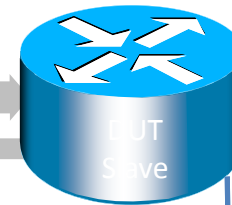
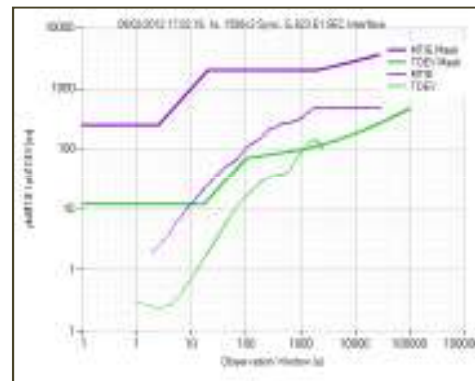
Metrics defined include;

- FPR, FPP, FPC - Floor delay packet population, ratio/percentage/count.
 - ***FPP Limits defined in G.8261.1***
 - ***1% of packets within 150μsec of floor delay in every 200sec period.***
 - Defined for networks transferring frequency.
 - MEF investigation the use of FPP to define SLA parameters.
- MATIE, minMATIE - Maximum Average Time Interval Error
- MAFE, minMAFE - Maximum Average Frequency Error
- minTDEV, PercentileTDEV, BandTDEV (TDEV – Time Deviation)
- ClusterTDEV
- pktfilteredTIE, pktfilteredMTIE, pktfilteredTDEV, pktfilteredFFO

Packet Metrics, example result

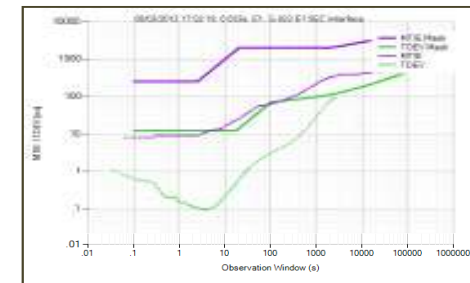


pkfilteredMTIE/TDEV on Sync:

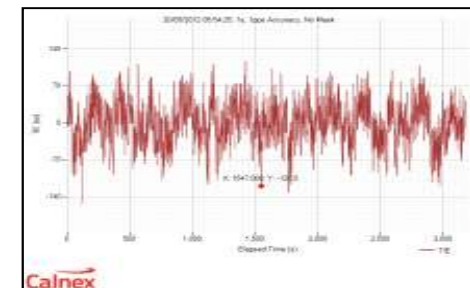


Frequency
Time/Phase

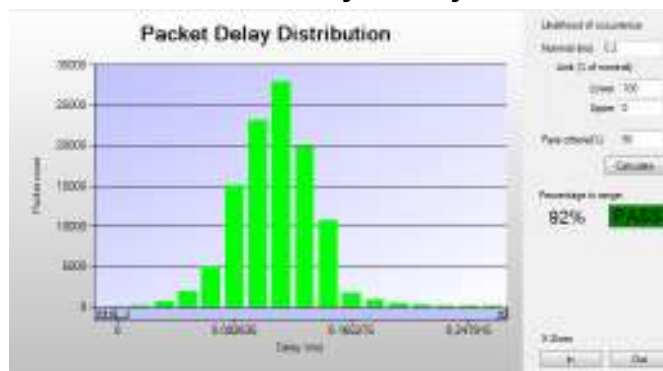
E1 MTIE/TDEV



1pps TIE



PDF - Probability Density Function



MAFE



Mask: NSN HRM-2

Summary of Evaluation Plan

When testing Time/Phase



Remember those
Measurement planes

- **SyncE**
 - Required when 1588v2 used with SyncE.
- **1588v2**
 - BC
 - TC
- **Ordinary Clocks**
- **Networks**
 - PoC, consider your own network topology and test to that.

- Standards in force.
- G.8262
 - Wander
 - Jitter
- G.8264
 - ESMC behaviour

- G.8273.2 Standard under development.
 - Time Noise Generation
 - Time Noise Tolerance
 - Time Noise Transfer
 - Phase Transient & Holdover;
- Consider behaviour during Traffic Congestion.

- Prove accuracy of CorrectionField.
 - Fixed Error, Variable Error, Asymmetry.
- IEEE Std C37.238-2011 'PTP in Power Systems Applications'
 - Profile specify $\leq 50\text{nsec}$.

- Characterise using G.8261 Appendix VI test cases.
- Measure
 - Frequency Accuracy.
 - Time Accuracy.

- Metrics specified in G.8260 Appendix I.
 - FPP, limit in G.8261.1
 - MAFE, minTDEV, etc
 - pktfilteredMTIE, pktfilteredTDEV
- Evaluate selected devices with Network.



CALNEXSOL.COM

Tommy Cook
tommy.cook@calnexsol.com
+44 (0) 1506-671-416