The Need for Speed and its impact on Sync.

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Contents

- The requirements for speed, high data rates, increased bandwidth
- The impact for the oscillator requirements to satisfy high data rates
- Frequency multiplication and phase noise
- High frequency oscillators for low jitter
- Subsequent possible impact on Oscillator performance for Sync requirements
- Meeting the challenge, Oscillator technology/advances, Examples

The need for Speed and its impact on Sync.

- **By speed we are referring to high speed data rates.**
  - Required to satisfy the exponential rise for greater and greater data rates.
- **By Sync. we are more specifically referring to the greater demands for time synchronisation.**
  - Microsecond and below phase/time stability requirements
- **Higher bandwidth, requires higher modulation rates or more complex modulation schemes**
  - Ethernet
    - Evolving from 1Gbit and 10Gbit to 25Gbit, 100Gbit and even 400Gbit.
  - High speed Optical communication, Coherent transceiver/receiver, 100Gbit
  - Air interface more complex modulation schemes, 16, 64 to 128 QAM
- **Imposes Requirements on the oscillator/oscillator chain**
  - Requirements for phase/time stability of <~100fs region over times of <~ 100us
  - Oscillator chain, frequency multiplied up to the carrier/modulation rate.
  - Requirement expressed in terms of Jitter or EVM specification.
  - Both an integral of phase spectral density over a bandwidth

Higher QAM Rates Require Better PN

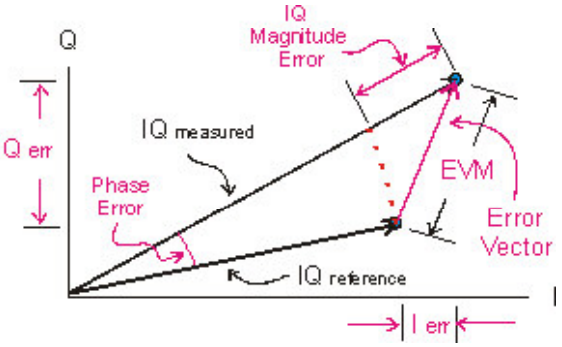
- **One way to increase bandwidth (Download/Upload speeds) is to increase QAM**
  - HSPA 16 to 64 QAM depending on signal strength
  - LTE 16 to 64 QAM depending on signal strength
  - LTE-A up to 128 QAM
- **As the QAM rate increases the more data they embed into the signal, the more precisely they have to measure the phase of each carrier signal**
  - This means that the phase noise(typically 100Hz to 100kHz) must be improved to meet the Error Vector Magnitude (EVM) masks.
  - e.g. EVM definition from 802.11b/g

$$EVM[n] = \sqrt{Ierr[n]^2 + Qerr[n]^2}$$

where [n] = measurement at the symbol time

Ierr = I Ref - I Meas

Q err = Q Ref - Q Meas



  - Poor phase noise means it's impossible to distinguish one code from another and the system is forced to reduce the QAM rate

Error Vector Magnitude - Example

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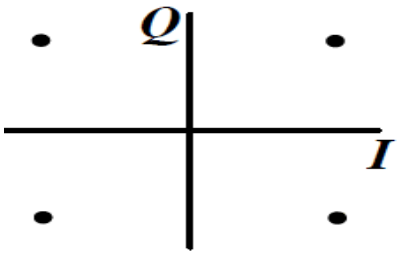
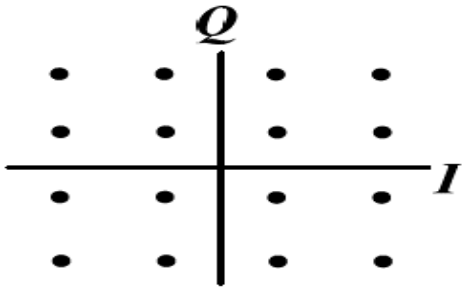
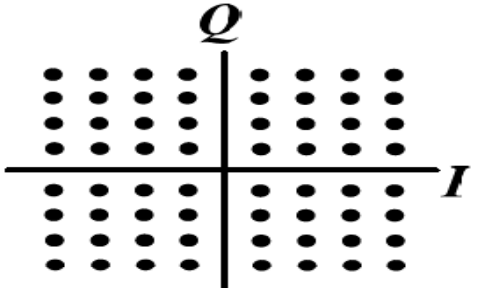
QPSK



16 - QAM



64 - QAM



More and more bandwidth = faster download/upload

Poor Phase Noise

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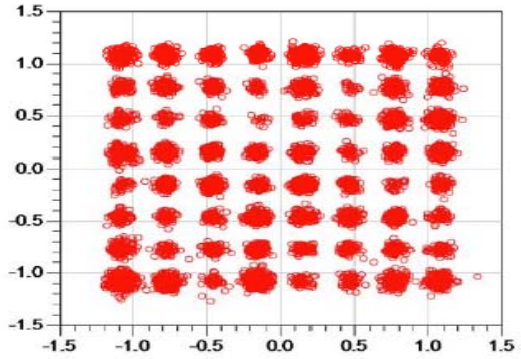
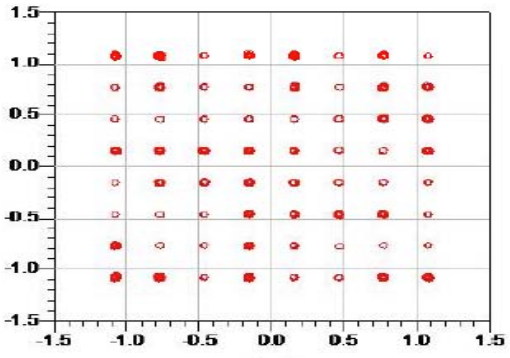
Harder to decode

EVM (dB)	EVM (°)
-28	2.28



EVM (dB)	EVM (°)
-40.2	0.56



Good Phase Noise

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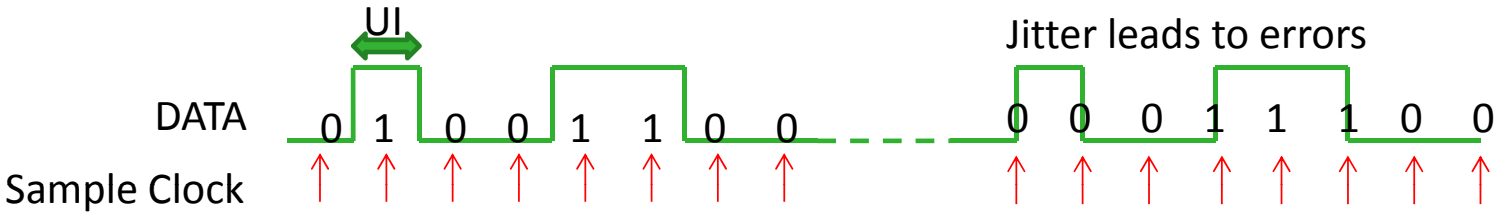
Easier to decode

Jitter specification – SyncE



- **Often Specified as peak-peak e.g. G.8262**
  - But normally measured as RMS jitter, for oscillator. BER 10^{-9} implies Pk-Pk ~ 12 * RMS
  - Total pk-pk jitter, transmit and receive, needs to be ~ less than 0.5UI (unit interval)

- **25G and 100G**
  - Requirement scales with Unit interval
  - Jitter specification for 25G and 100G needs to be 40 and 100 times better than 1G requirement
  - ~1ps and 250fs
  - Base oscillator contribution needs to be significantly less than this.

Table 6 – Synchronous Ethernet jitter generation for EEC-Option 1 and EEC-Option 2

Interface	Measuring filter	Peak-to-peak amplitude (UI)
1G (Notes 1, 2, 4)	2.5 kHz to 10 MHz	0.50
10G (Notes 1, 3, 4)	20 kHz to 80 MHz	0.50

NOTE 1 – There is no specific high-band jitter requirement for synchronous Ethernet. The relevant IEEE 802.3 jitter requirements shall be met in addition to the specific synchronous Ethernet wideband jitter requirements specified in this table. [IEEE 802.3] defines measurement methodologies. The applicability for those measurement methodologies in a synchronization network environment is for further study.

NOTE 2 – 1G includes 1000BASE-KX, -SX, -LX; multi-lane interfaces are for further study.

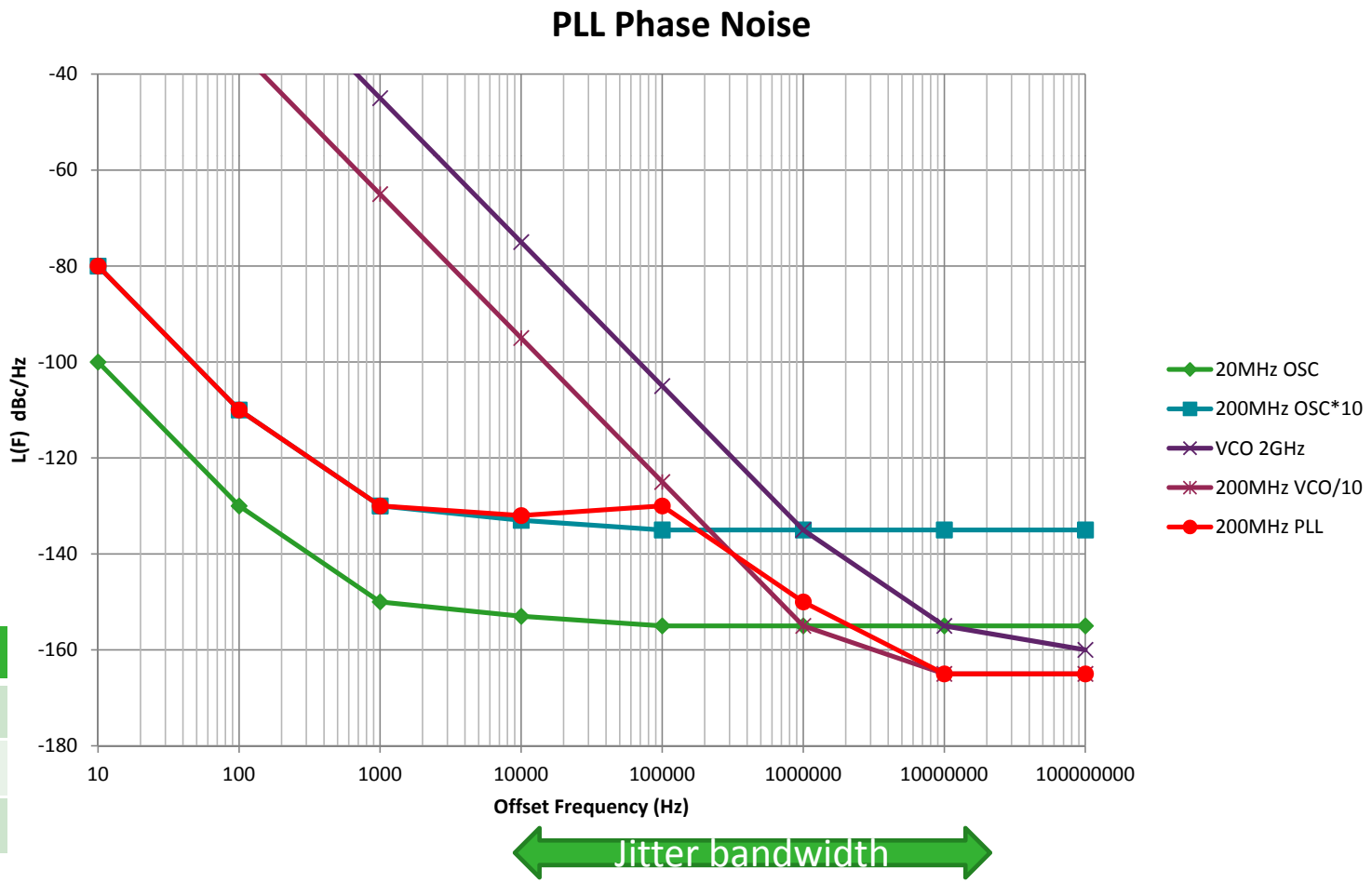
NOTE 3 – 10G includes 10GBASE-SR/LR/ER, 10GBASE-LRM, 10GBASE-SW/LW/EW; multi-lane interfaces are for further study.

NOTE 4 – 1G: 1 UI = 0.8 ns
10G (10GBASE-SR/LR/ER, -LRM): 1 UI = 96.97 ps
10G (10GBASE-SW/LW/EW): 1 UI = 100.47 ps

Oscillator chain - Multiplying the frequency up

- **Idealised example**
- **Locking high frequency VCO to low frequency crystal oscillator**
  - Example 200MHz output from 20MHz TCXO and 2GHz VCO
    - TCXO 20MHz
    - TCXO * 10
    - VCO 2 GHz
    - VCO /10
    - 200MHz PLL output

Oscillator	Jitter 10kHz- 20MHz (ps)
TCXO	0.89
VCO	1.41
PLL	0.17

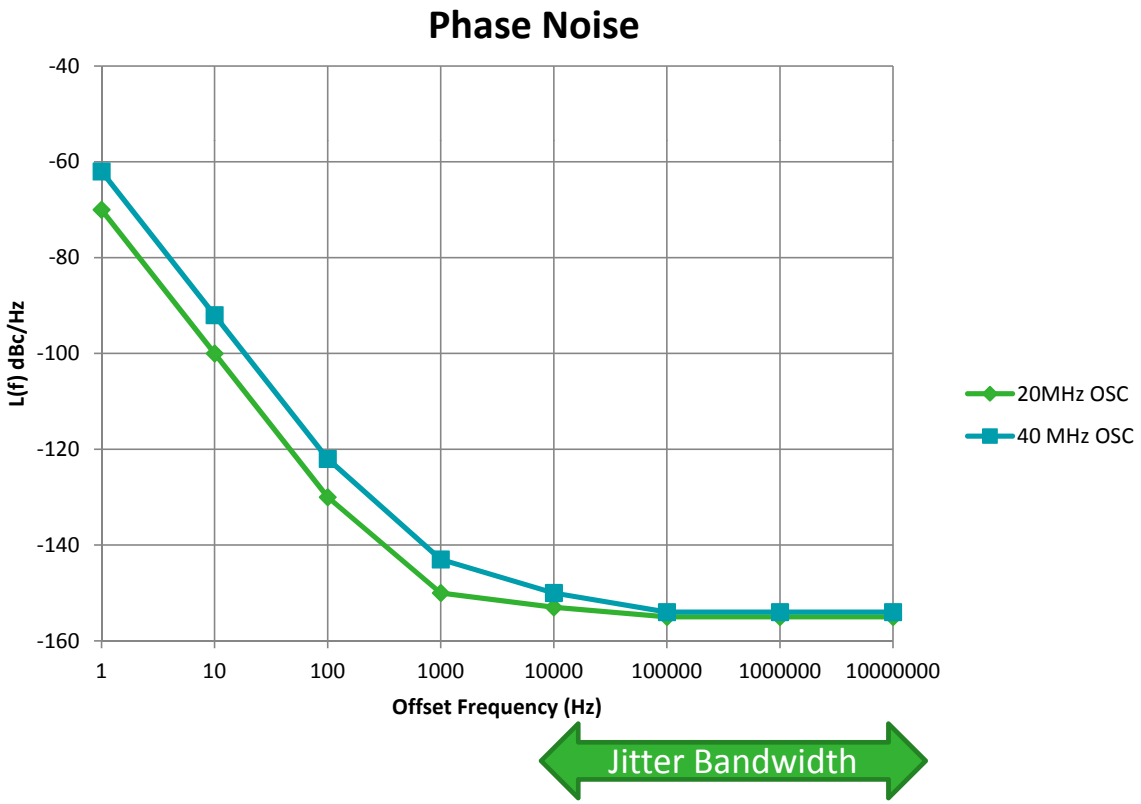


Multiplying the frequency up

- **Jitter stays the same with idealised frequency multiplication/division.**
  - Phase noise increases 20log(M) ideally. Where M is frequency multiplication.
  - Integral of noise over a bandwidth, is in radians.
  - converting from radians to time is scaled by frequency, so jitter remains the same.
- **Lower frequency oscillator only contributes up to loop bandwidth**
  - Up to ~ 100kHz on previous example
  - Lower loop bandwidth, higher Q VCO, reduces jitter of composite PLL output
- **May have multiple loops**
  - GHz VCO, locked to high frequency VCXO, locked to low frequency TCXO/OCXO
  - Trend to save costs to remove high frequency VCXO and go directly from TCXO/OCXO to GHz VCO

How to improve Oscillator Jitter

- **Higher Frequency Oscillator.**
  - Noise floor stays low, as oscillator frequency increases, so less jitter.
  - Jitter 10kHz to 20MHz
    - 20MHz Osc, 0.89ps
    - 40MHz Osc, 0.5ps
- **Integral of Phase noise.**
  - Jitter bandwidth matches noise floor
  - Double sideband or phase spectral density = 2*single sideband (L(f))
  - Integral gives noise relative to 1 radian, need to multiply by period/2π to convert to Jitter in seconds.
- **Double the Oscillator frequency with the same noise floor results in half the jitter.**



Challenges with higher frequency oscillators

- **Increasing Quartz frequency- by making the Quartz thinner**
  - Thinner Quartz, more susceptible to mass transfer and Stress
    - Increased aging and hysteresis
  - Also tends to lead to a smaller Quartz blank. Relative size tolerances harder to control.
    - Increased perturbations due to interfering modes.
    - Can take a long time to perfect a new design, especially for TCXOs.
  - Angle tolerance on thinner blank is more difficult, co-planarity etc.
    - Increased tolerance on the frequency temperature slope at oven set point, degrades performance in OCXO.
- **Using overtone Modes:-**
  - Normally fundamentals for TCXO's and 3rd Overtones for OCXO's
  - Third Overtone (traditionally used for OCXO's)
    - Three times thicker for same frequency as fundamental, better aging
    - Higher Q, better short term stability
    - But nine times less pullable
      - TCXO and especially VCTCXO devices require extra external components, hyper-abrupt varactor, inductors and larger crystals.
      - Larger oscillator packages and more costly.

Impact on Sync. from oscillator perspective

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- **So we have 10's of femtoseconds stability over 10's of microseconds at one end and 1 microsecond stability for hours at the other end of the stability spectrum**
- **The requirement for both time and frequency synchronisation**
  - Frequency stability in the few ppb range
  - Requirements for sub microsecond stability over time periods of minutes to hours
  - Requires higher stability oscillators
    - lower aging for time holdover
    - Better frequency temperature stability for longer time constant synchronisation loops.
      - Loop bandwidth moving to 50 to 100mHz for IEEE1588 supported networks
      - Loop bandwidth requirements for 1mHz or less for unsupported or partially supported networks
- **But Higher frequency oscillators are naturally less stable**
  - Aging increases at least linearly, probably more with frequency
  - Poorer frequency temperature stability
    - TCXO perturbations
    - OCXO angle tolerance
  - Higher load, supply, acceleration sensitivity etc.

Meeting the Challenge

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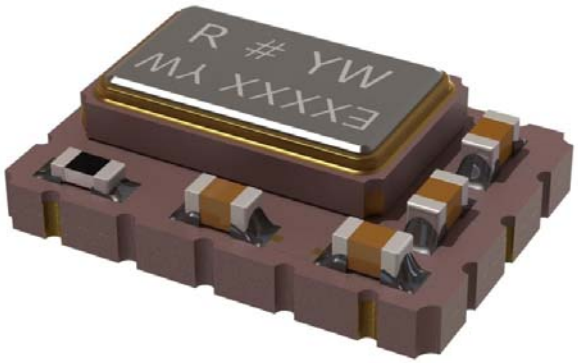
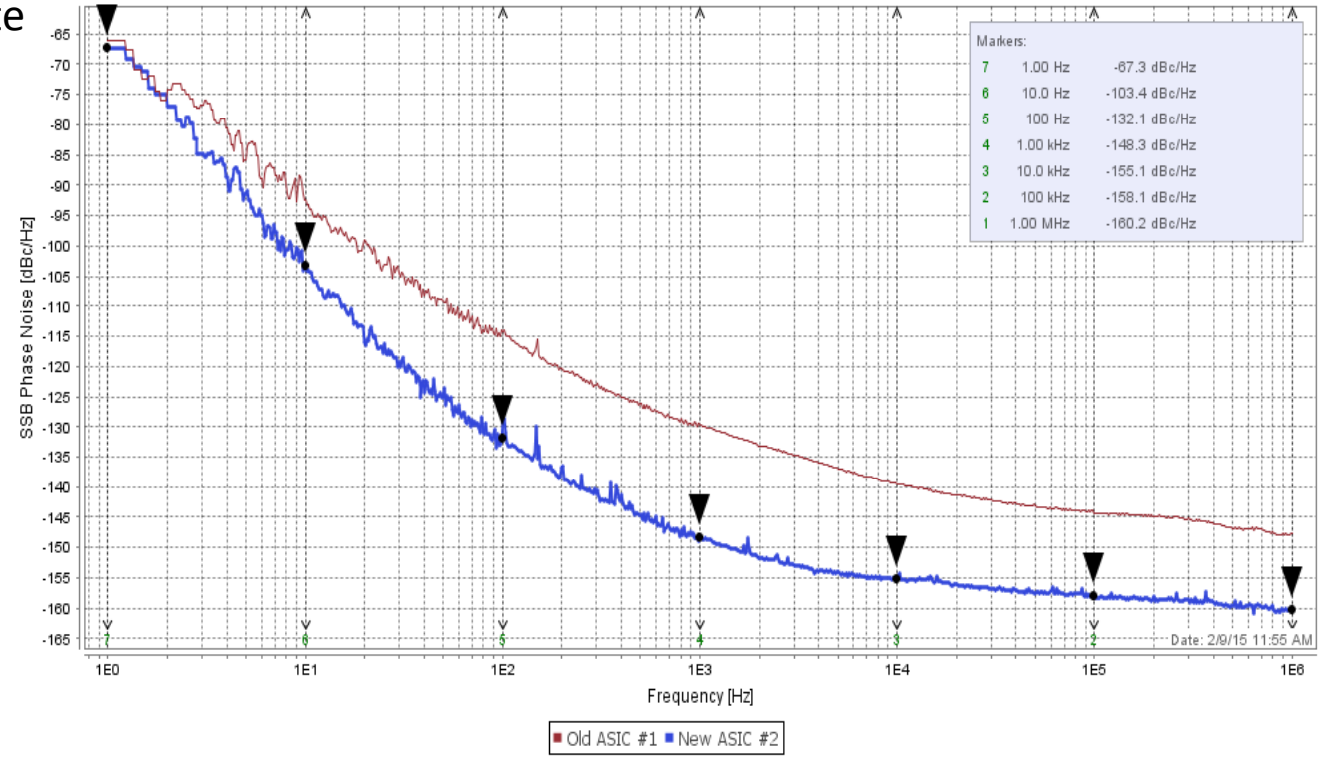
- **What is required:-**
  - Need to either reduce the jitter of high stability low frequency oscillator
  - Or Increase stability of high frequency low jitter oscillator
  - Or both
- **How:-**
  - Redesign the TCXO or OCXO ASIC, second/third generation ASIC's
    - Reduces noise floor from ~-150dBc/Hz to nearer ~ -160 dBC/Hz, jitter reduction~ 3 times
  - Enhance stability with digital control and processing.
    - Digital temperature compensation on top of analogue compensation/control
    - Digital aging compensation, requires reference or aid of system
  - Better PLL chips
  - Modules incorporating low noise high stability oscillator, digital control and low noise frequency multiplication PLL.

New generation TCXO ASIC

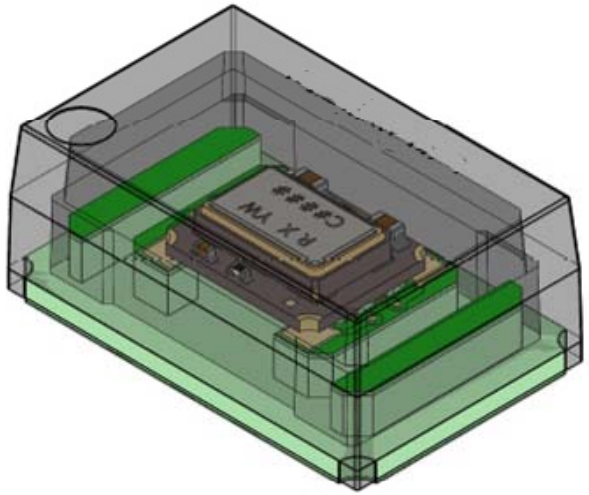
- **Circuit redesign and capacitors added for compensation filtering and power supply noise reduction**
- **Note :- CMOS Buffer converts amplitude noise on the power supply to phase noise on the signal**
  - Speed of buffer gate is dependent on supply voltage
  - Variable delay through buffer gate
  - Creates white phase noise
  - So noise floor degrades
  - Jitter increases

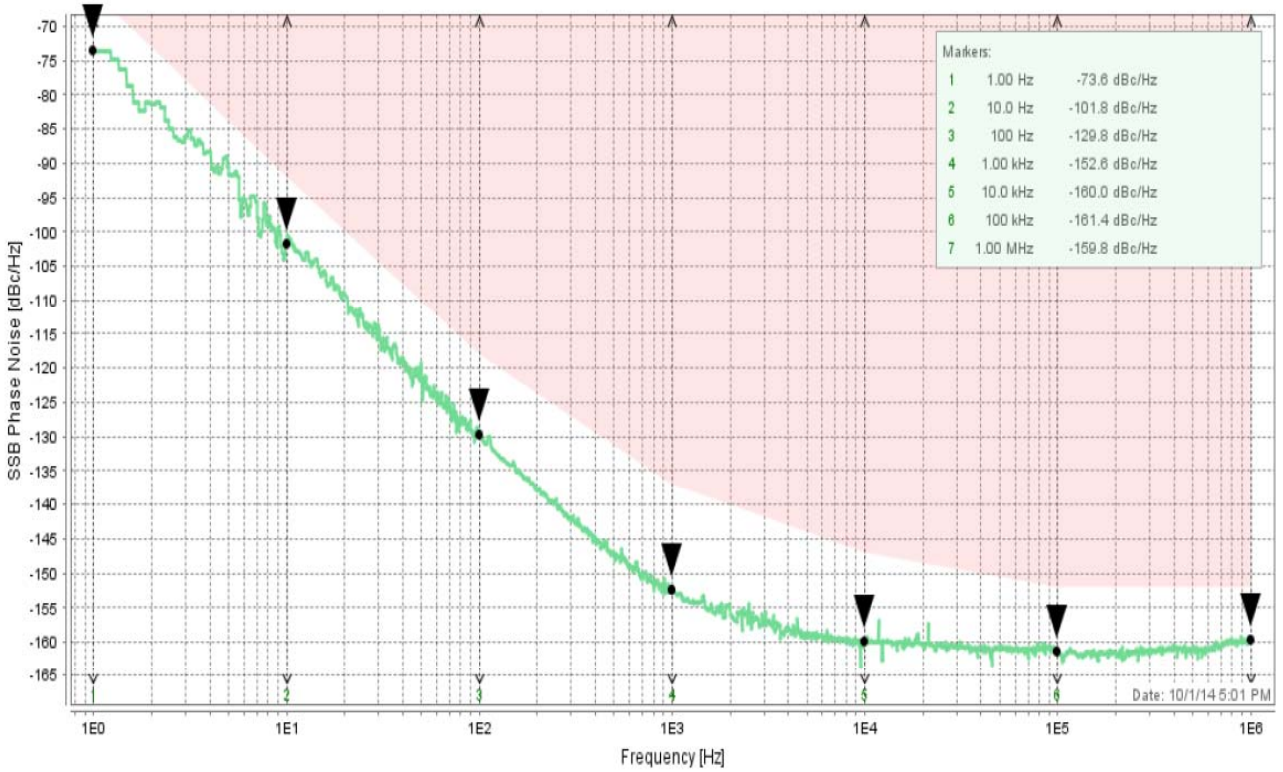




Next generation Miniature OCXO ASIC

- **Example of miniature OCXO ASIC development shaded area shows previous typical noise for the same 20MHz fundamental strip crystal. Green measurement is next generation ASIC**





Digital enhancement of analogue system

- **High resolution digital frequency control**
  - Frequency step size should be similar magnitude or less than the noise, 10^{-11} to 10^{-12}
  - Implies need for 20 bit monotonic DAC ($1.048576*10^6$ steps)
- **For temperature compensation medium resolution digital temperature measurement**
  - 12 to 16 bit ADC
  - Needs to measure the effective oscillator/crystal temperature, not always the same as ambient.
    - OCXO requires the internal crystal temperature, ~proportional to power dissipation.
    - TCXO needs the temperature sensor closely coupled.
- **For Aging compensation, a frequency reference is required**
  - Can be implied from frequency adjustment record, when device is in locked mode
  - Calculated from comparing to supplied frequency reference, when locked.
    - Needs to be aware of system state, locked, holdover, when to go into holdover mode.

System Compensation vs Oscillator Level

- **Some temperature and/or aging compensation can/has been done at system level**
- **Advantages of system level approach**
  - For aging, particularly the system has effective record of oscillator frequency error with time.
  - Information on locked/holdover mode, quality of service.
- **Disadvantages of system level approach**
  - Difficulty separating aging and temperature effects.
    - Ambient temperature not a good measurement of OCXO crystal temperature
      - Airflow effects, change in airflow can be equivalent to 10 of degrees temperature change.
    - Any thermal lag between temperature sensor and crystal introduces errors during temperature change, dynamic effects.
  - Voltage control of oscillator, very sensitive to
    - Power supply, earth reference errors due to large change in OCXO supply current with temperature.
    - High stability voltage reference required for DAC, and/or temperature coefficient needs calibrating out for optimum holdover.

Effect of digital post compensation TCXO

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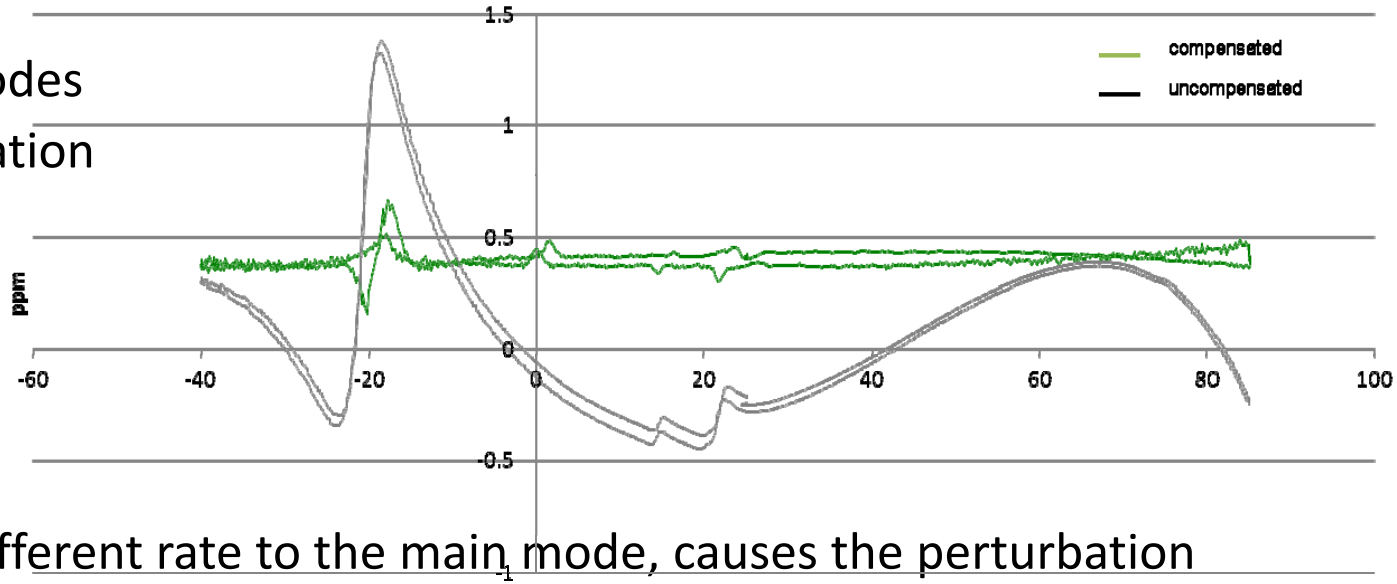
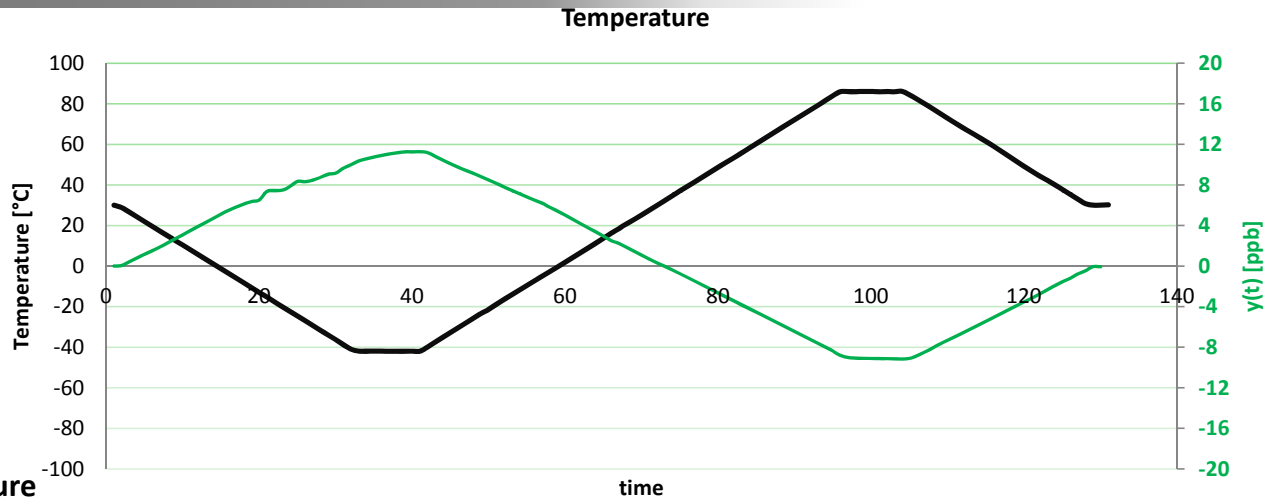
- **Higher frequency crystals tend to suffer from perturbations**
  - Example (blue line)shows frequency excursion after analogue compensation, large perturbation ~ +/- 0.75ppm
  - Interference from coupled modes
  - Adding extra digital compensation
    - Post analogue comp.
    - Green line
  - Frequency stability improved
    - ~ +/-0.2 ppm

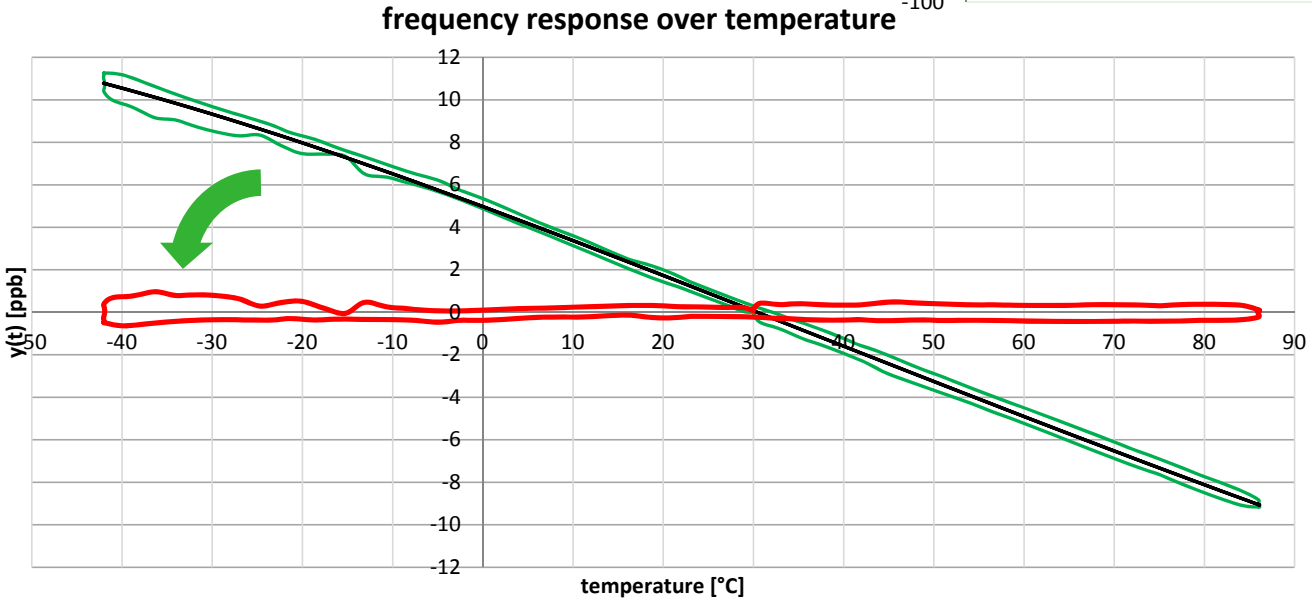


- **Perturbations move with time!**
  - Coupled mode can age at a different rate to the main mode, causes the perturbation to effectively move in temperature. Digital post compensation could be severely degraded. If it does not adapt/learn during lifetime.

OCXO holdover – temperature compensation

- **Temperature compensation procedure**
  - Apply temperature profile
  - Evaluate frequency variation
  - Then apply digital compensation algorithm

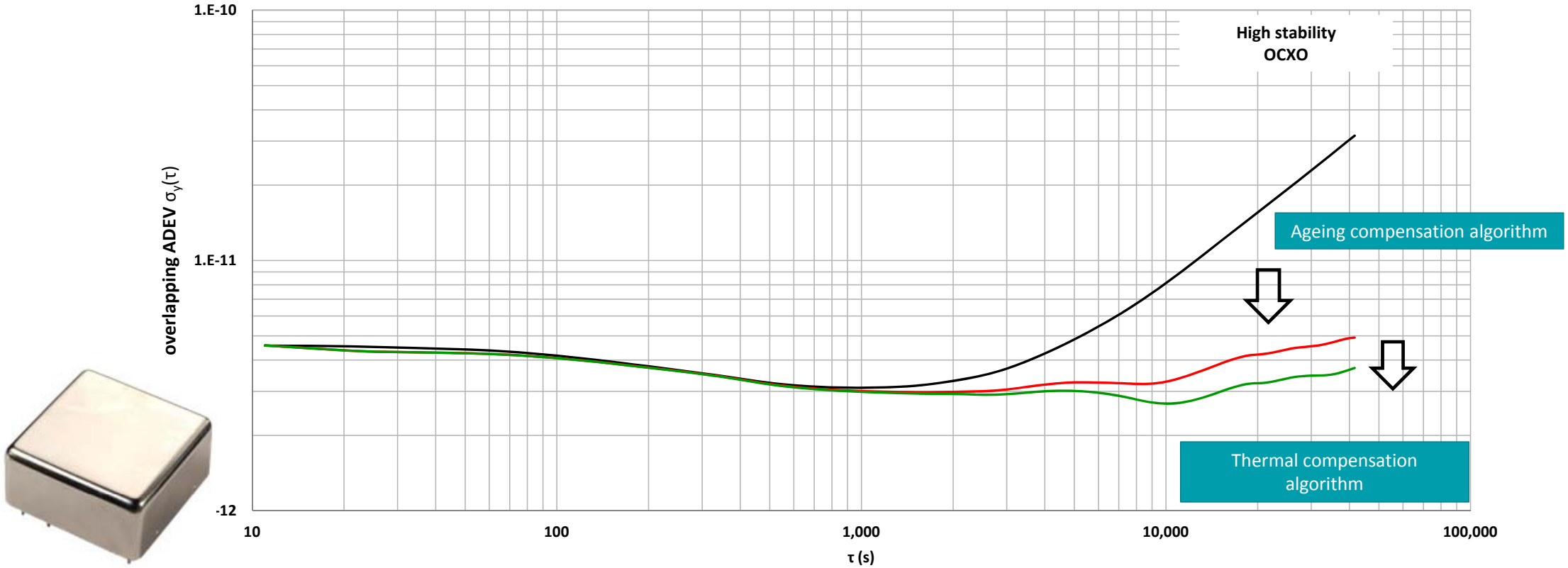




- But…Oscillator hysteresis limits the residual error

OCXO holdover –Ageing and temperature compensation

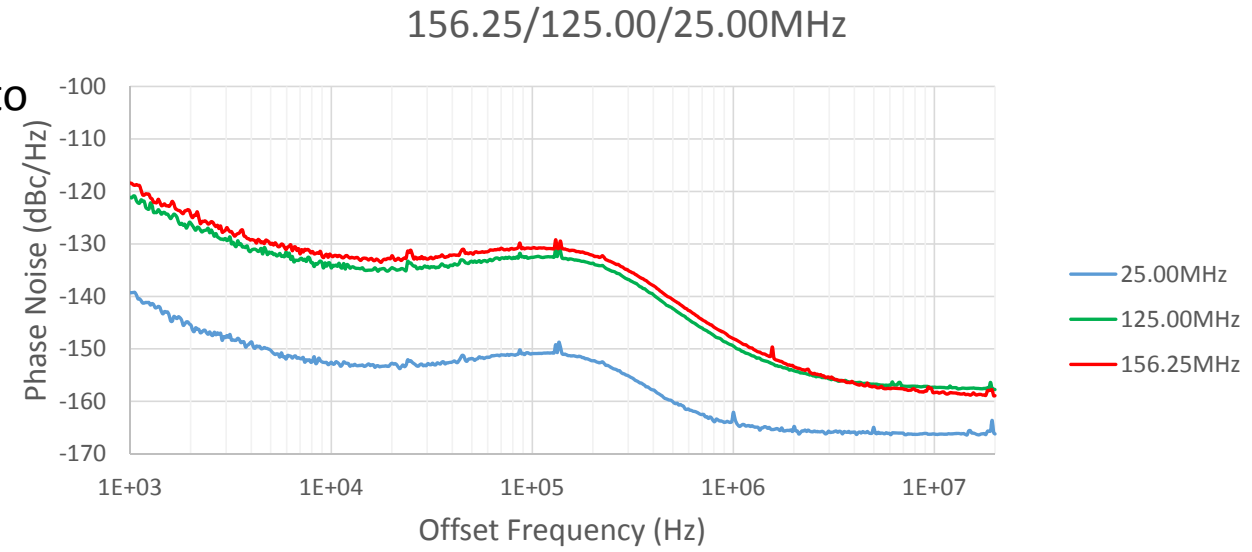
- **Frequency stability over time, represented by Allen Deviation.**
  - Sub 10^{-11} region over hours, achieved with digital ageing and temperature compensation



Oscillator Module

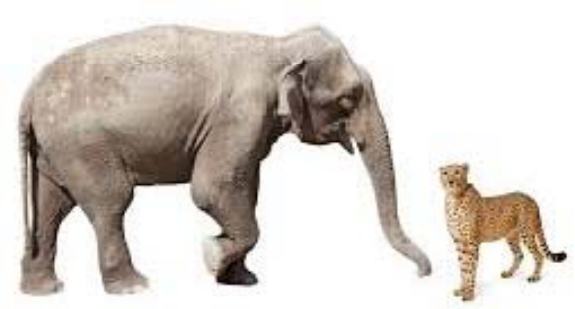
- **Module incorporating**
  - High resolution Digital Frequency Control (I2C/SPI)
  - High stability TCXO or OCXO
  - Low noise synthesizer with Low jitter outputs
    - <300 fs 12k-20MHz
    - Multiple outputs
    - Single sided and differential output types
- **Guarantees Higher Performance**
  - Reduces inter-component contributors to noise and frequency instability
  - Tested integrated performance
- **Enables digital enhancement**
  - Temperature compensation
  - Ageing compensation

Example Configuration Performance



Summary

- **Combination of low jitter for high data rates and high stability for very good time synchronisation is a challenge**
- **Advances are being made**
  - Improved ASIC, crystal and oscillator design.
  - Digital enhancement for temperature and ageing compensation.
  - Improved PLL chips
- **But stability takes time!!**



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