Metrology and Tools for Interoperability Testing of Precision Time Protocol (PTP) in Power Systems Communication Networks

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NIST Smart Grid Program

Workshop on Synchronization and Timing Systems
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What is the UCAIug IEC 61850 Interoperability Plugfest?

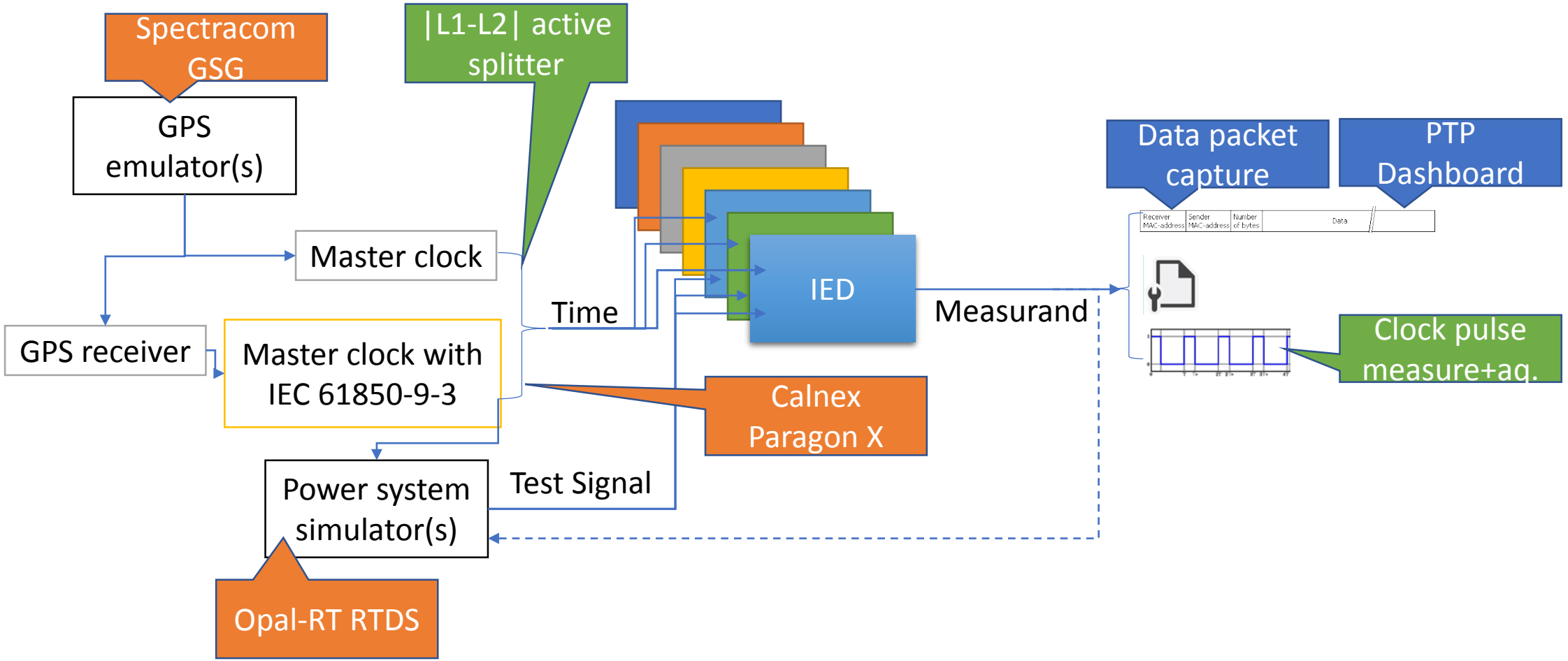
Objective: Identify issues related to the interoperation of substation automation equipment from different vendors.

- Interoperation has been identified as an impediment to adoption of modern sensors, relaying and control equipment.
- All profess to comply to the **IEC 61850** Substation communication protocol.
- Sponsored by UCAIug
- Several parallel testing events:
  - **Integrated Application**
  - **Time Sync**
  - Cyber Security
  - Substation Configuration Language (SCL)
  - **GOOSE and R-GOOSE**
  - **SV and R-SV**
  - **MMS**
- Recreate both *normal* and *stressed* environments?
- Over 208 attendees including system integrators, vendors, and utilities

Devices being tested

- PDC/ SCADA
- PMU/ AMU
- Relay
- IED
- TC/BC
- GPS receiver
- Clock

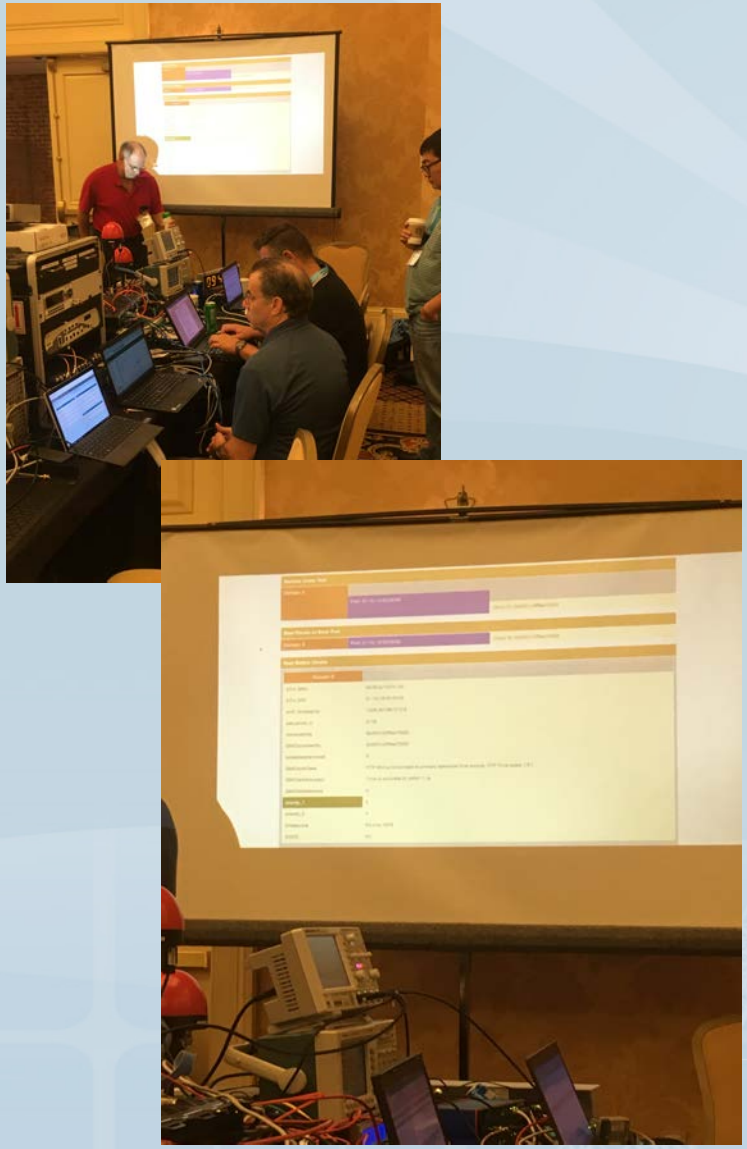
Test Equipment Provided By NIST



Why was NIST interested?

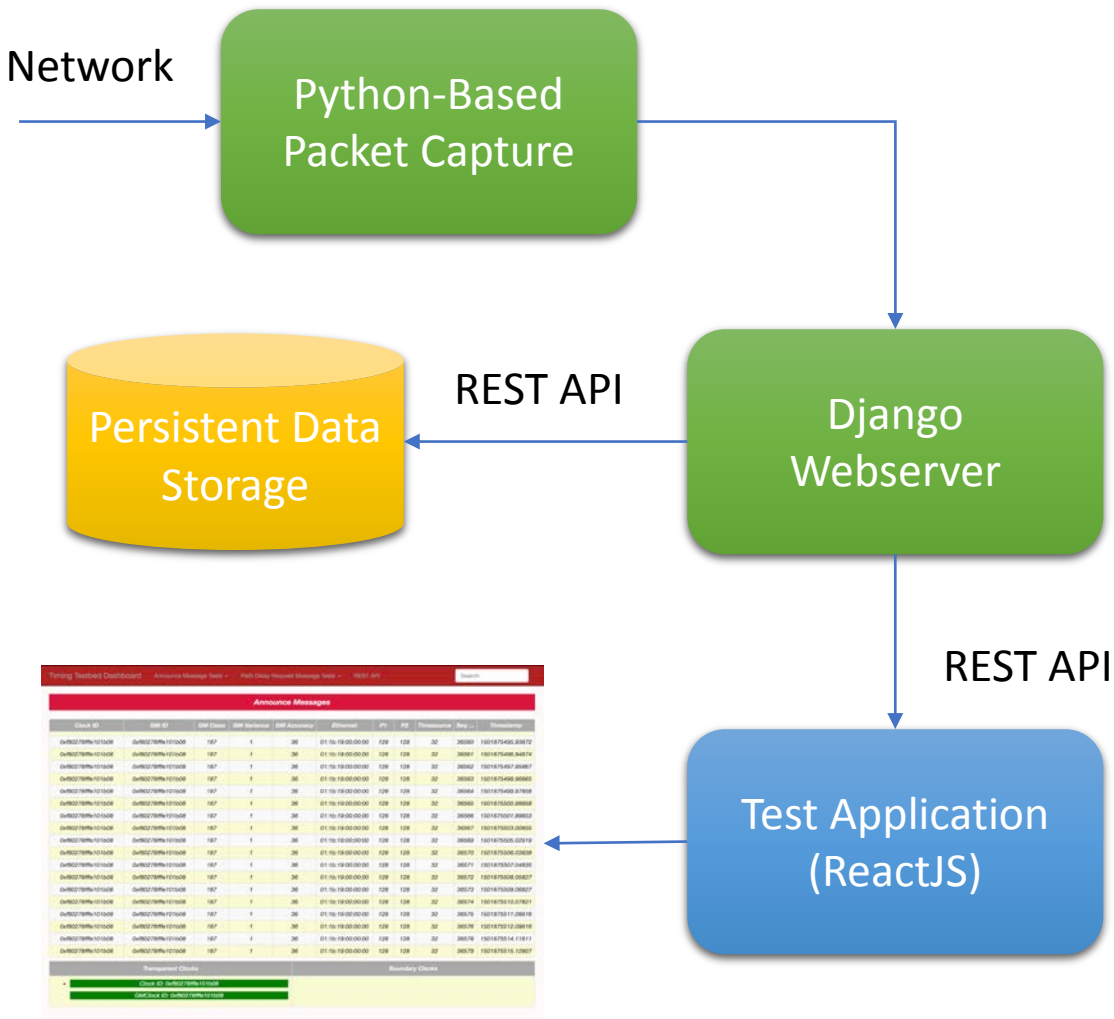
- Advancing interoperation is a state goal of the SGCPS program
- Metrology for these advanced systems require custom tools
- Engagement with industry on implementation issues tends to be hard
- Interop events highlight standards ambiguities
- Industry interest in testing and certification is difficult to gauge
- Peer pressure inspires participation with best of breed equipment
- NIST test capability in the area had not been benchmarked against industry leading practice

Time Sync Dashboard



- Versatile web application that can be viewed in any web browser on any platform
- Displays grandmaster tests in real-time
- Very generic and compatible with almost any operating system and web browser
- Easy to expand due to modular software design

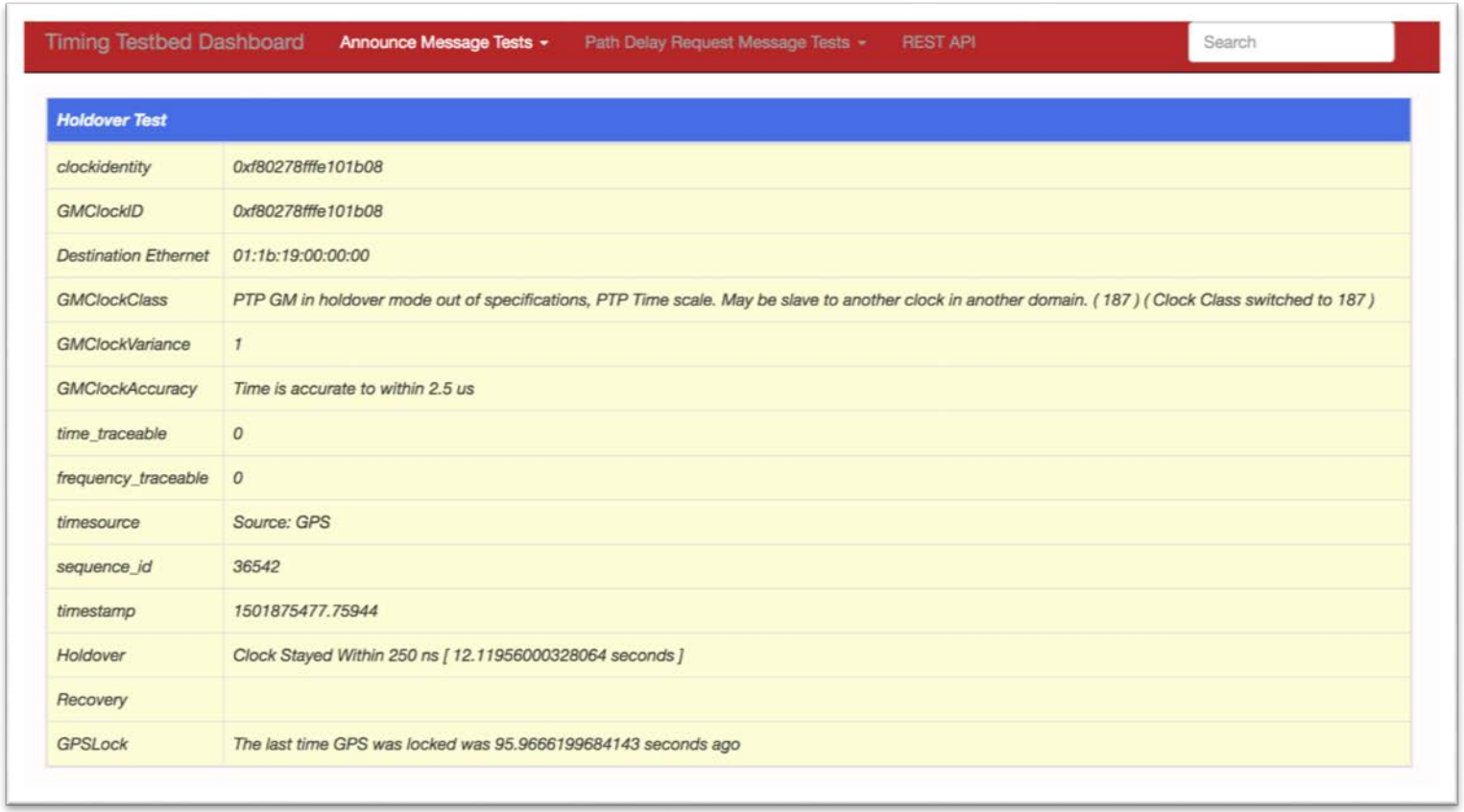
Dashboard Highlights



- Discovers PTP devices on the network
- Python-based Django web application to capture and display PTP packets
- Uses multi-threaded processing to have the web server and the packet capture work simultaneously.
- Supports common tests such as BMCA, Holdover, Positive and Negative Leap Second, Path Delay Request Messages, and Alternative Time Offset TLVs
- Displays incoming announce messages and pertinent fields and lists transparent and boundary clocks in real-time
- Database backend for persistent storage of device information and test data.

How it was used at the event

- Enabled users to focus on the pertinent PTP attributes of interest to determine if a device passed the conformance tests.
- Allowed Testers to see if Announce Messages were coming from the correct clock and whether they were reaching every part of the network
- Computes holdover time to log the duration of time a device is in each class
- BMCA test showed which comparison the algorithm made its decision on and whether the grandmaster clock was on the correct domain



Future expansion:

Scaling application to substation scale, enable remote monitoring, implement as a web service, integrate commercial test equipment

Orthographic view of Integrated test rack (Cuong for scale)

PTP Dashboard

|L1-L2| active splitter

Spectracom GSG

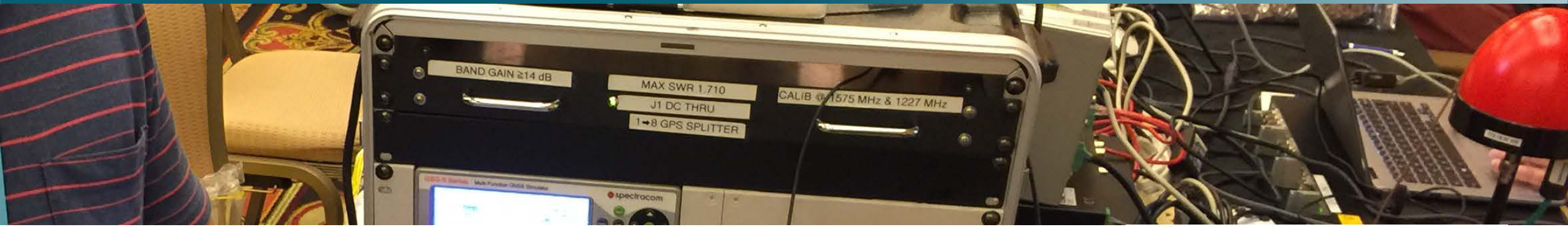
Calnex Paragon X

Clock pulse measure+ag.

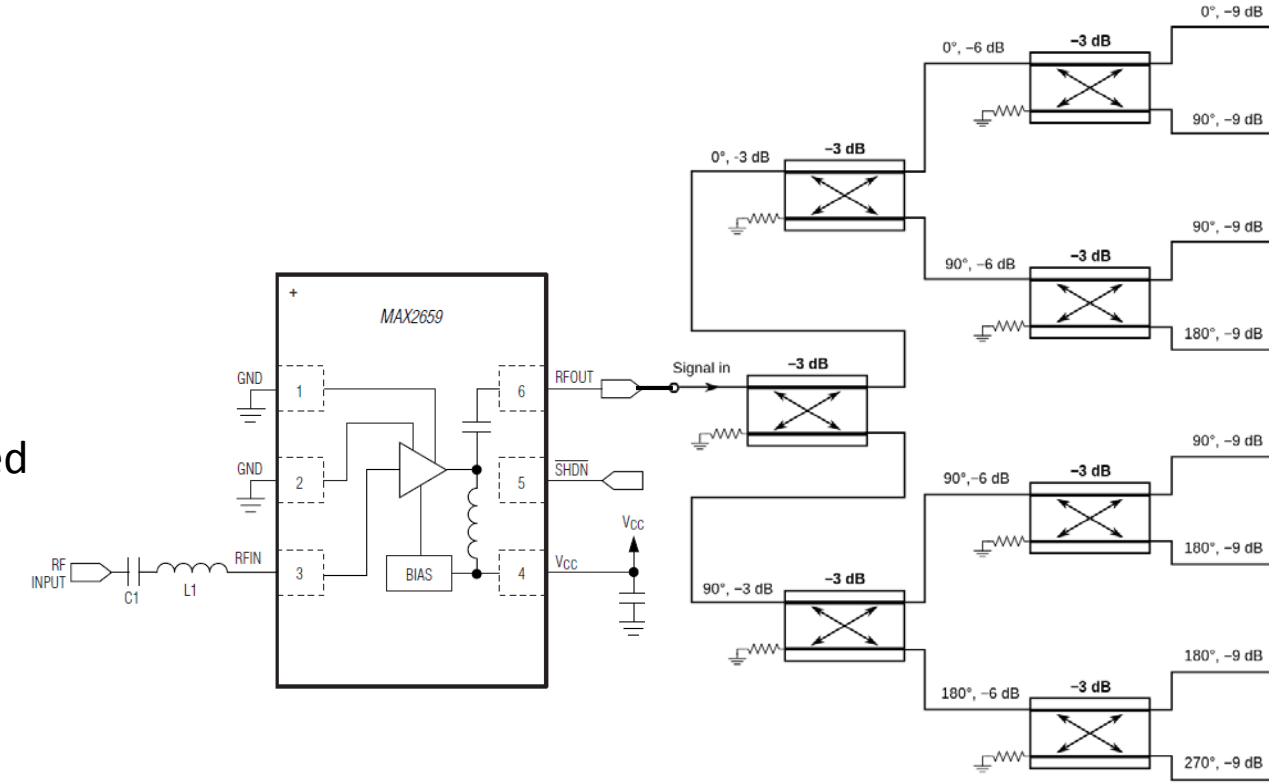
Opal-RT RTDS

- Baseline GPS conditions (variable sig strength)
- ± Leap second
- Radio hygiene

1X8 active splitter: 1 GPS source -> 8 receivers



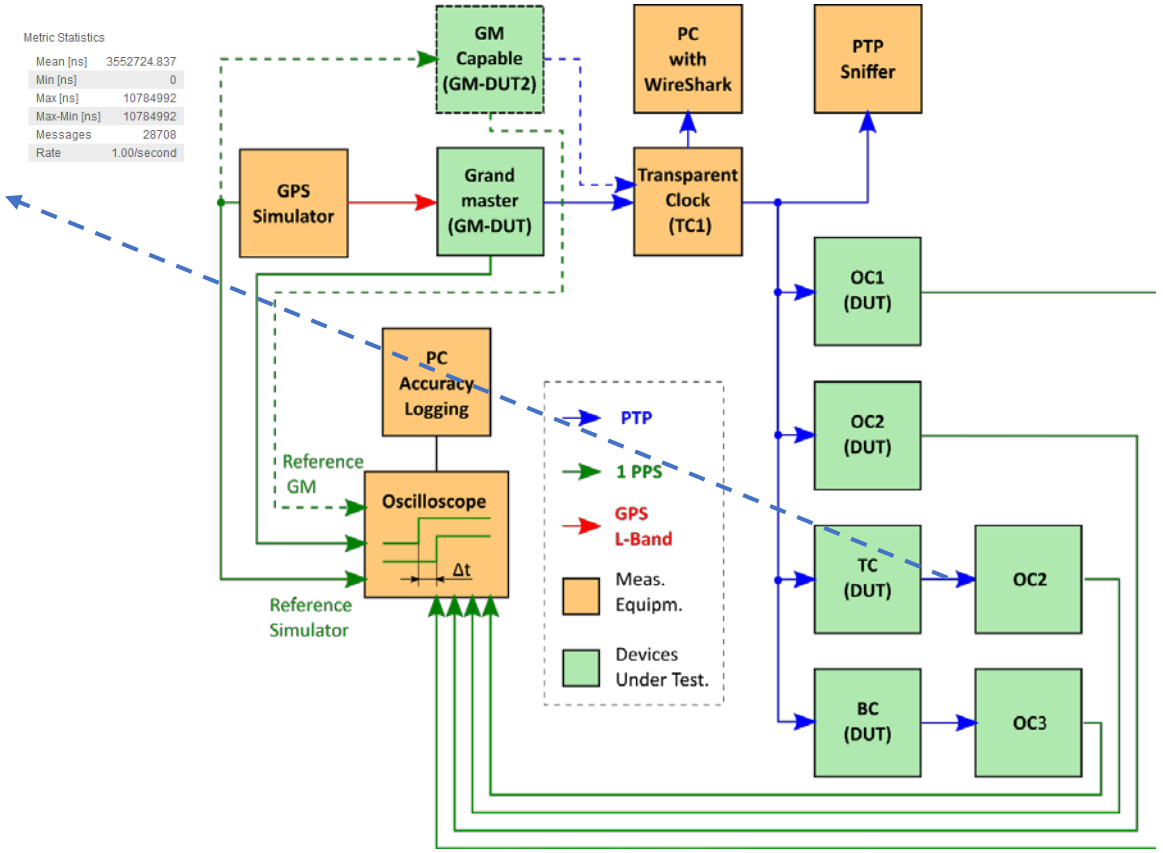
- MA11M Military Qualified Amplifier
- Channel Gain ≥ 14 dB
- SWR ≤ 1.7
- Calibrated at L1(1575MHz) and L2(1227MHz)
- 200Ω@0Hz dummy load on each port
- Does not need power injector (parasitic on P1)
- Uses a fully passive impedance network from Navtech.
- Remaining ports are impedance matched and DC blocked
- Phase matched ≤ 1°



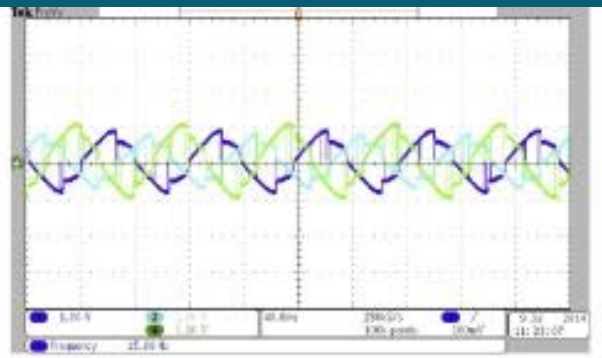
Calnex Paragon-X timing traffic profiler

Metric Statistics

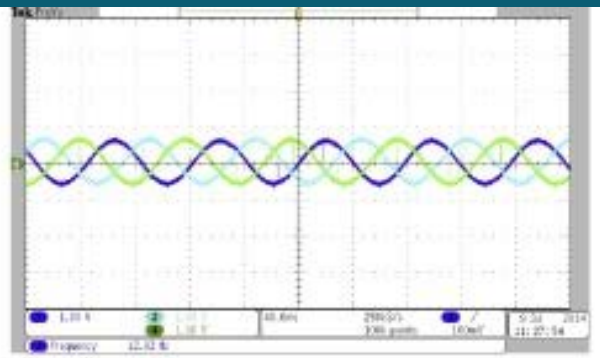
Mean [ns]	3552724.837
Min [ns]	0
Max [ns]	10784992
Max-Min [ns]	10784992
Messages	28708
Rate	1.00/second



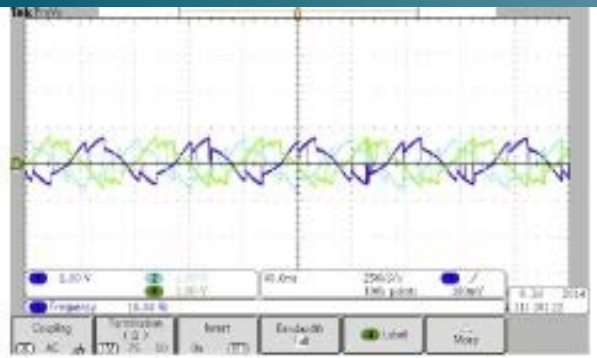
Time locked HiL simulation



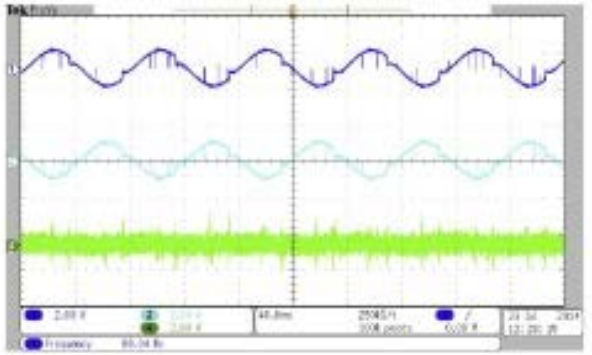
(a) 3 Phase Unbalanced Load Current



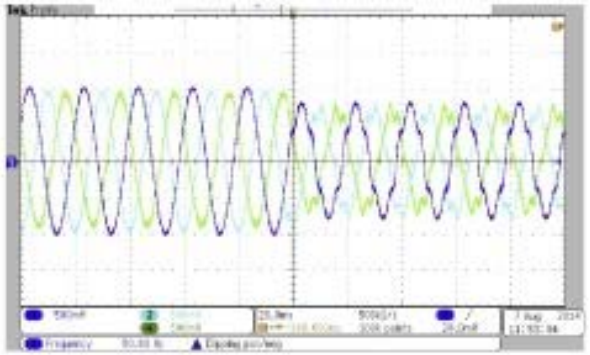
(b) 3 Phase Balanced Source Current



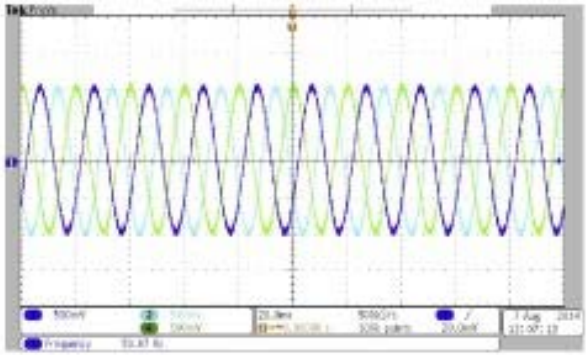
(c) 3 Phase Compensating Current



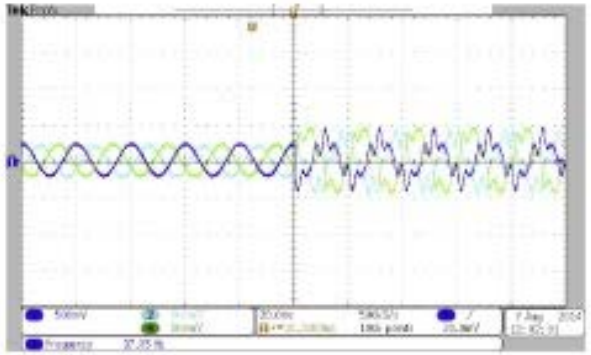
(d) Load, Compensating & Source Neutral Current



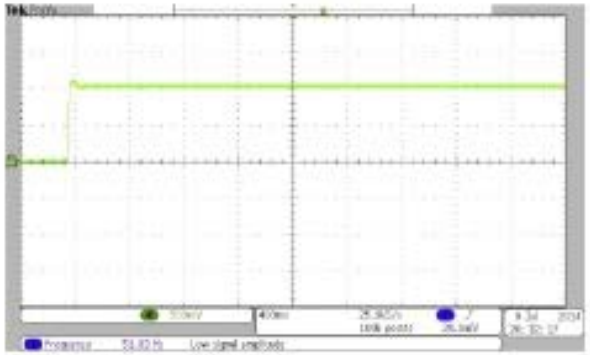
(e) 3 Phase Source Voltage



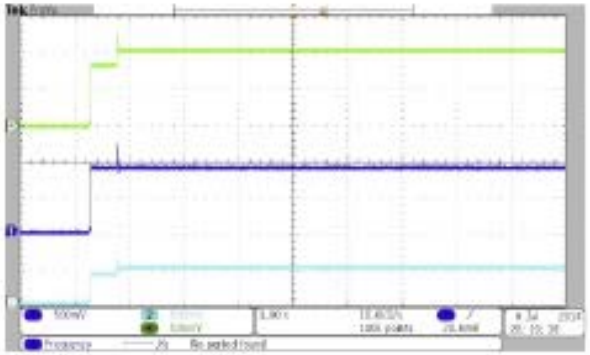
(f) 3 Phase Load Voltage



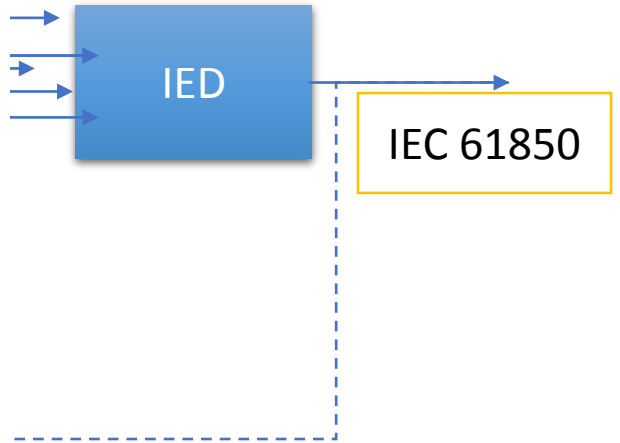
(g) 3 Phase Series Injected Voltage



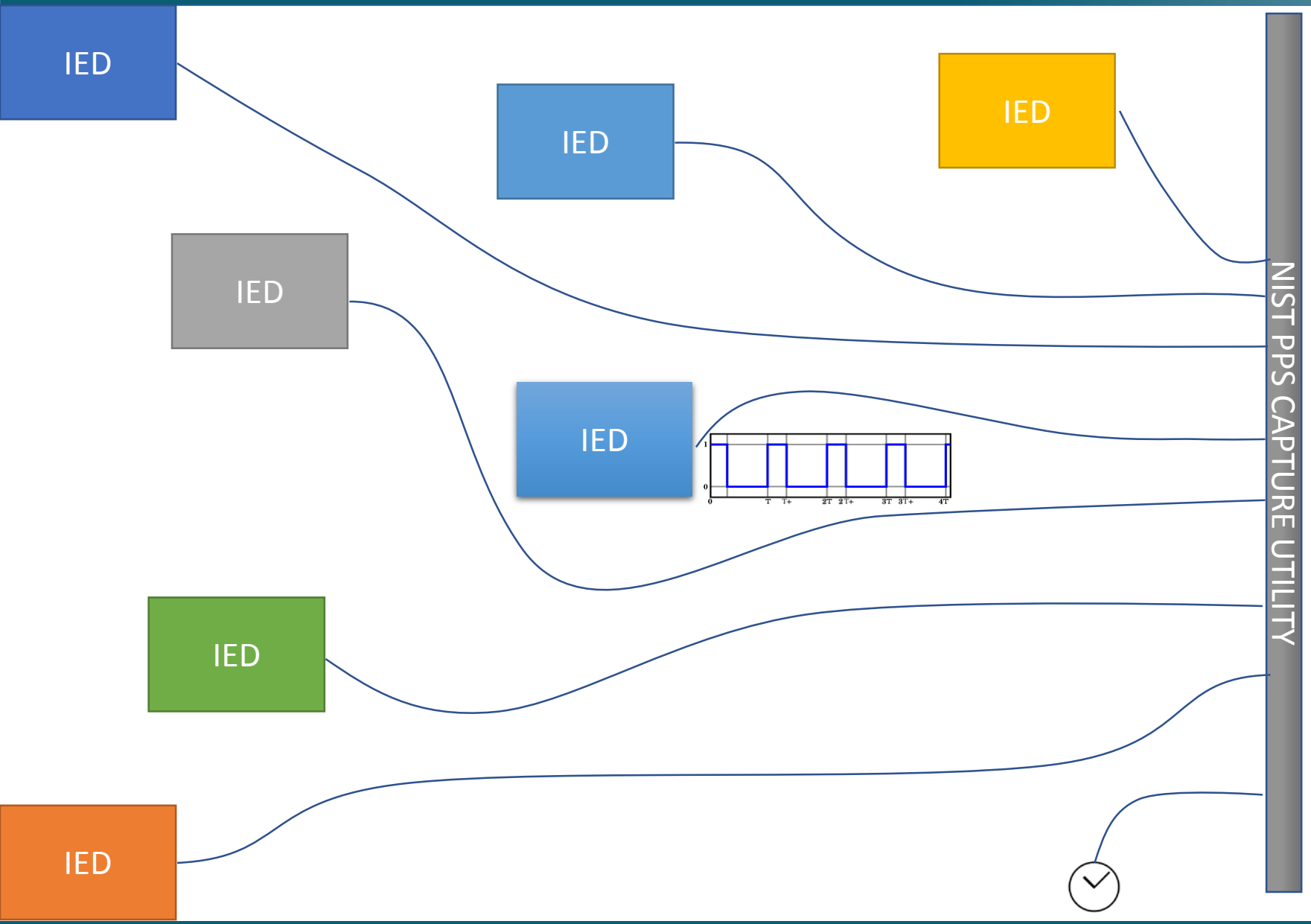
(h) DC Link Capacitor Voltage



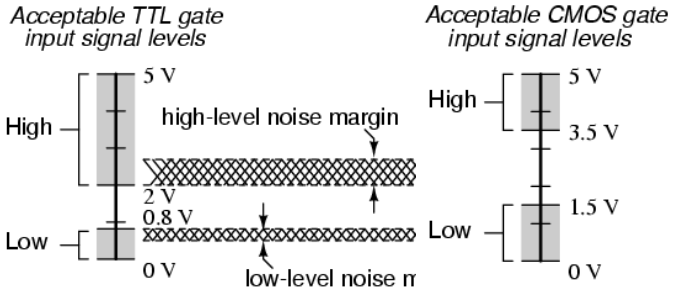
(i) Load, Shunt APF & Series APF Reactive Power

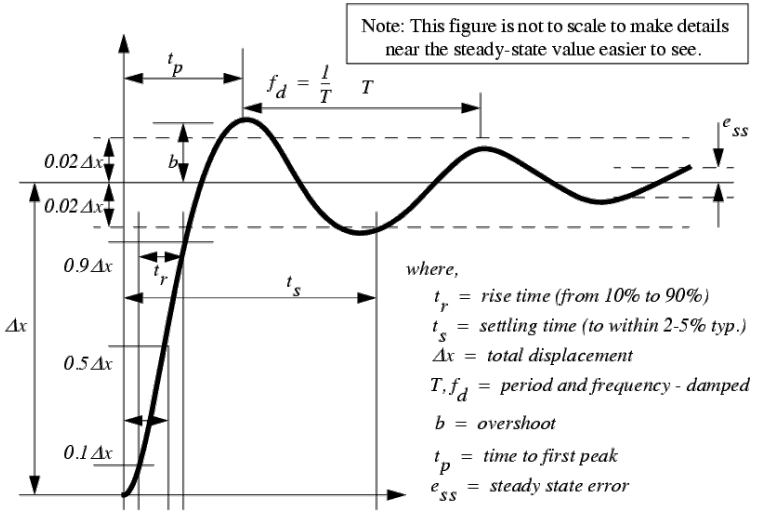


Pulse edge time error measurement

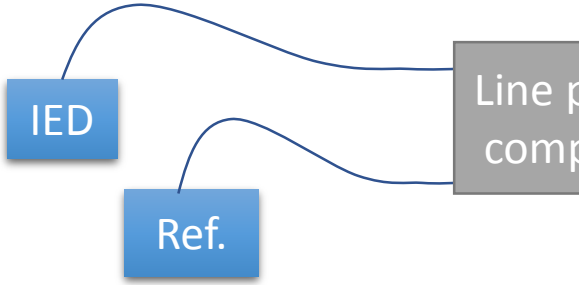


- Cable lengths [1-20] mts.
- TTL and CMOS logic
- Source impedances 50-10M
- 2nS resolution (traceable)
- Measure 8 channels
- Log data





Pulse edge time error measurement



Line parameter compensation

Front end impedance matching+ logic level selection

Low jitter edge detection

Time alignment

Acquisition triggering

Multichannel A/D

Visualization / Logging

- Cable lengths [1-20] mts.
- TTL and CMOS logic
- Source impedances 50-10M
- 2nS resolution (traceable)
- Measure 8 channels
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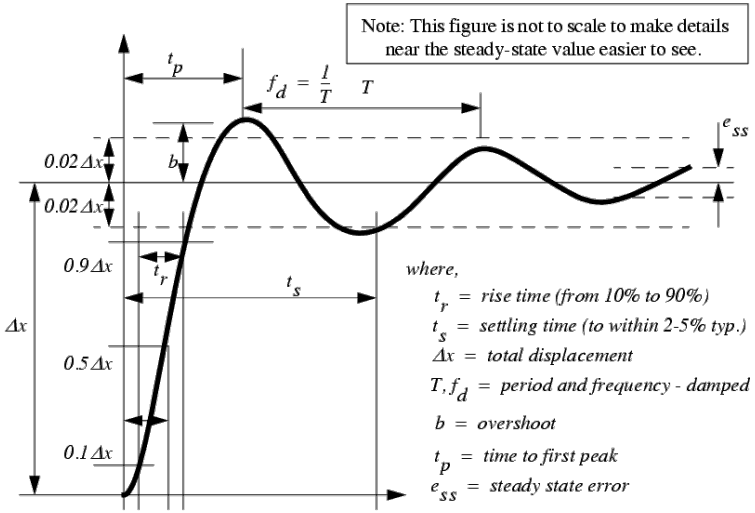
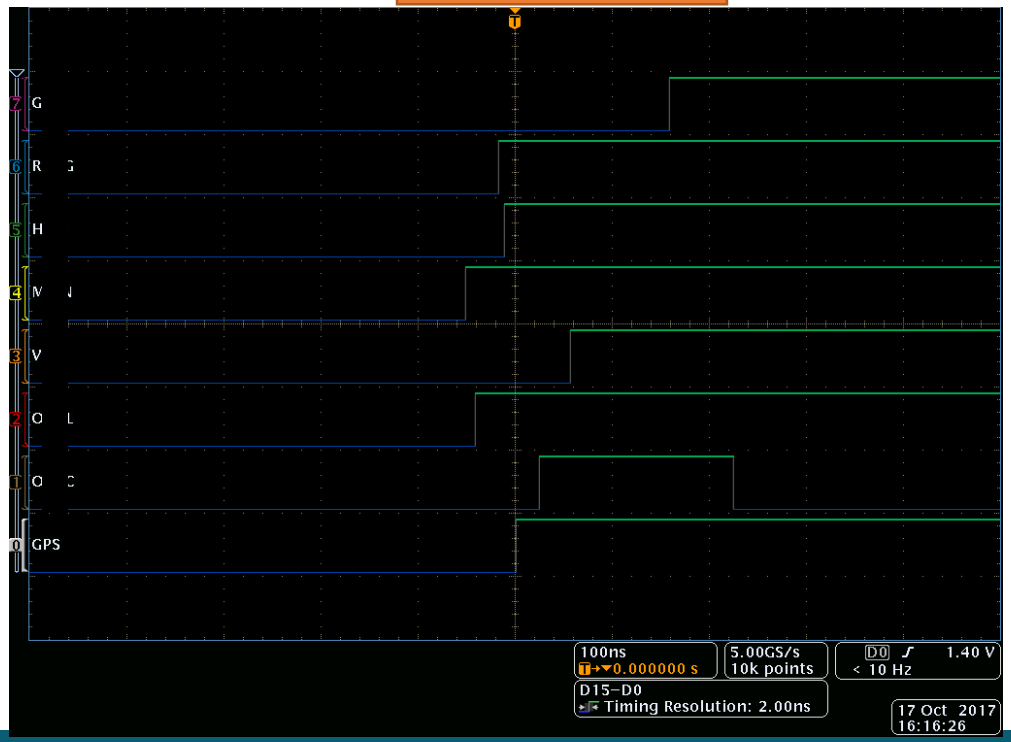
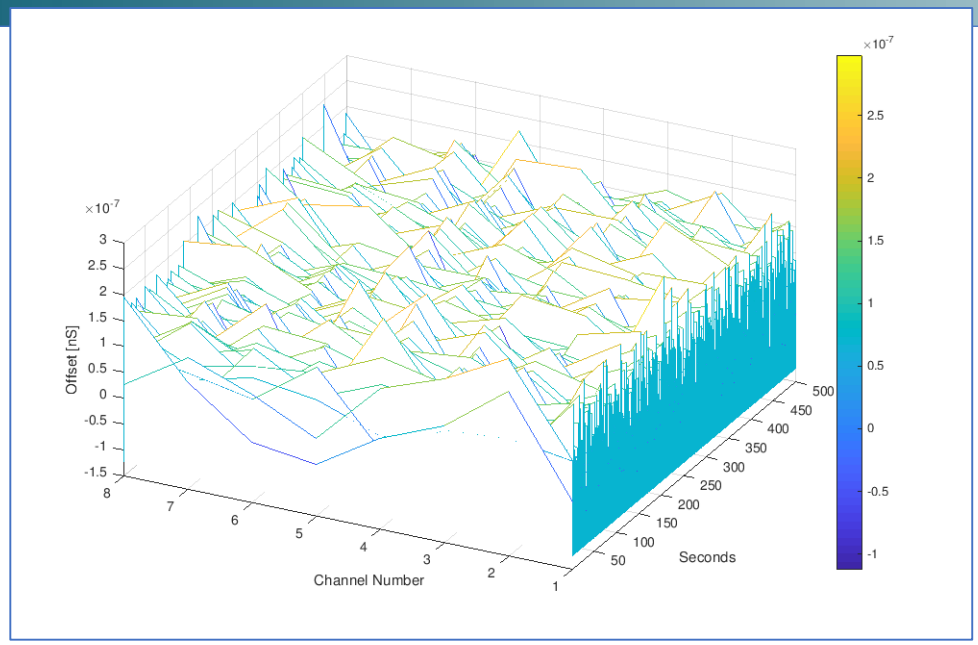
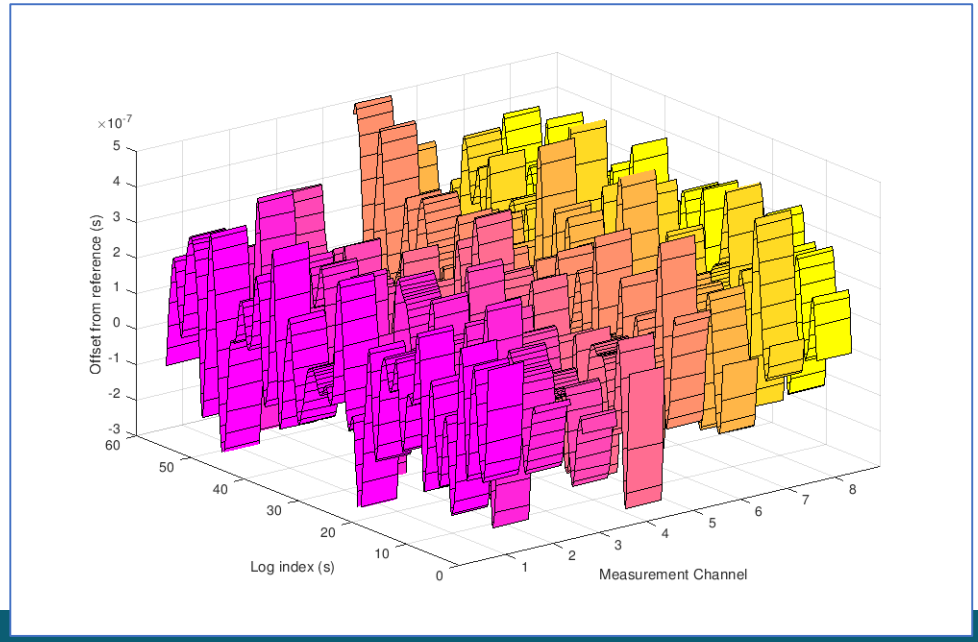




PPS Variations

- PPS capture utility provided 1E-8 second high resolution measurements of the behavior of each slave clocks in the test network
- These charts highlight sample cases of the type of analysis this tool may be used for
  - The top chart provides a view of the dynamic state of a synchronization network
  - The bottom chart is an interpolation fit using a 2nd order PLL model that provides visual illustration of the dynamics of synchronization within each clock even when the system is nominally at steady state





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Thank you!