Power Matters.

Microsemi

Distributed Time Services in Real Network Deployments

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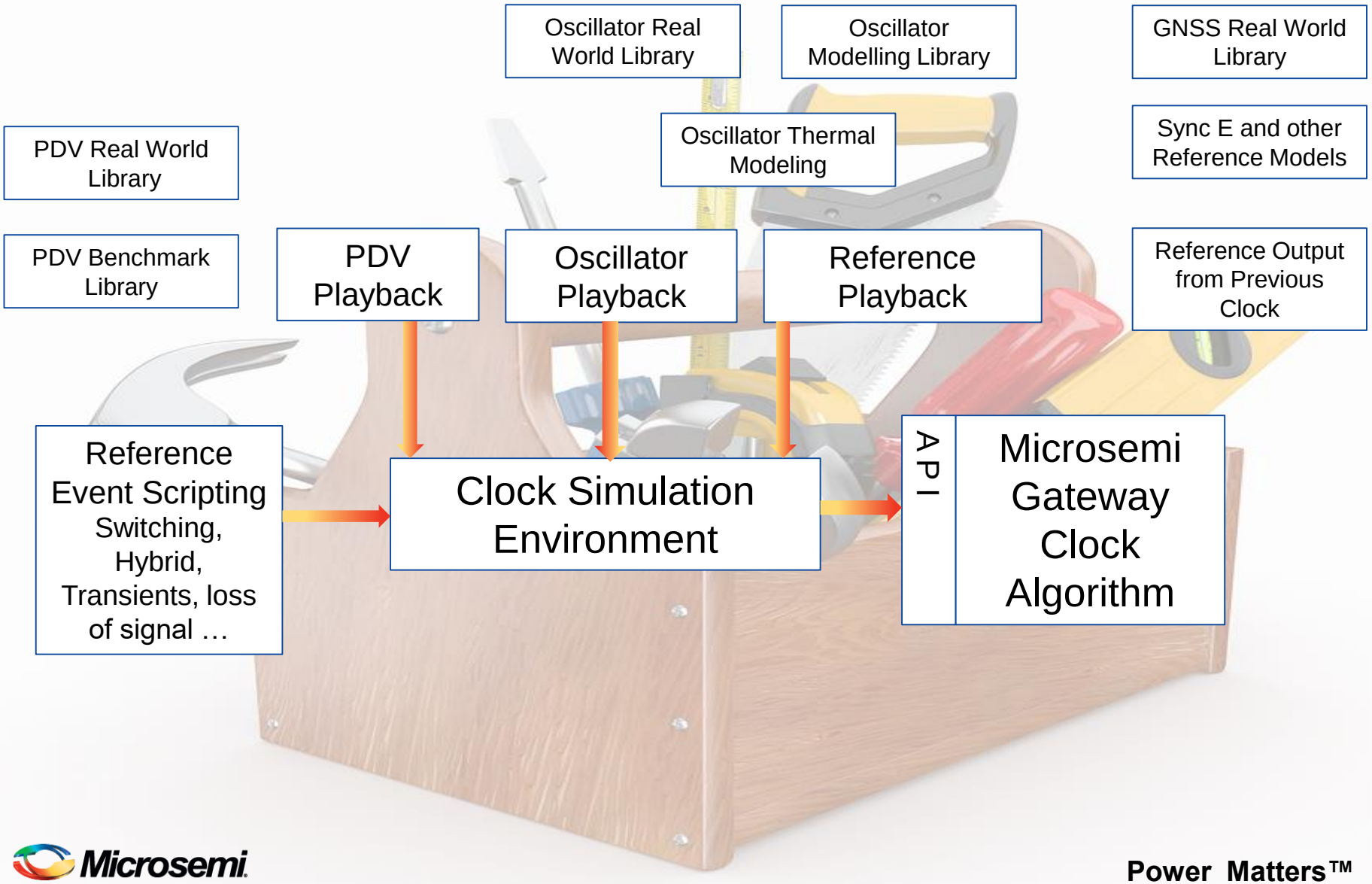
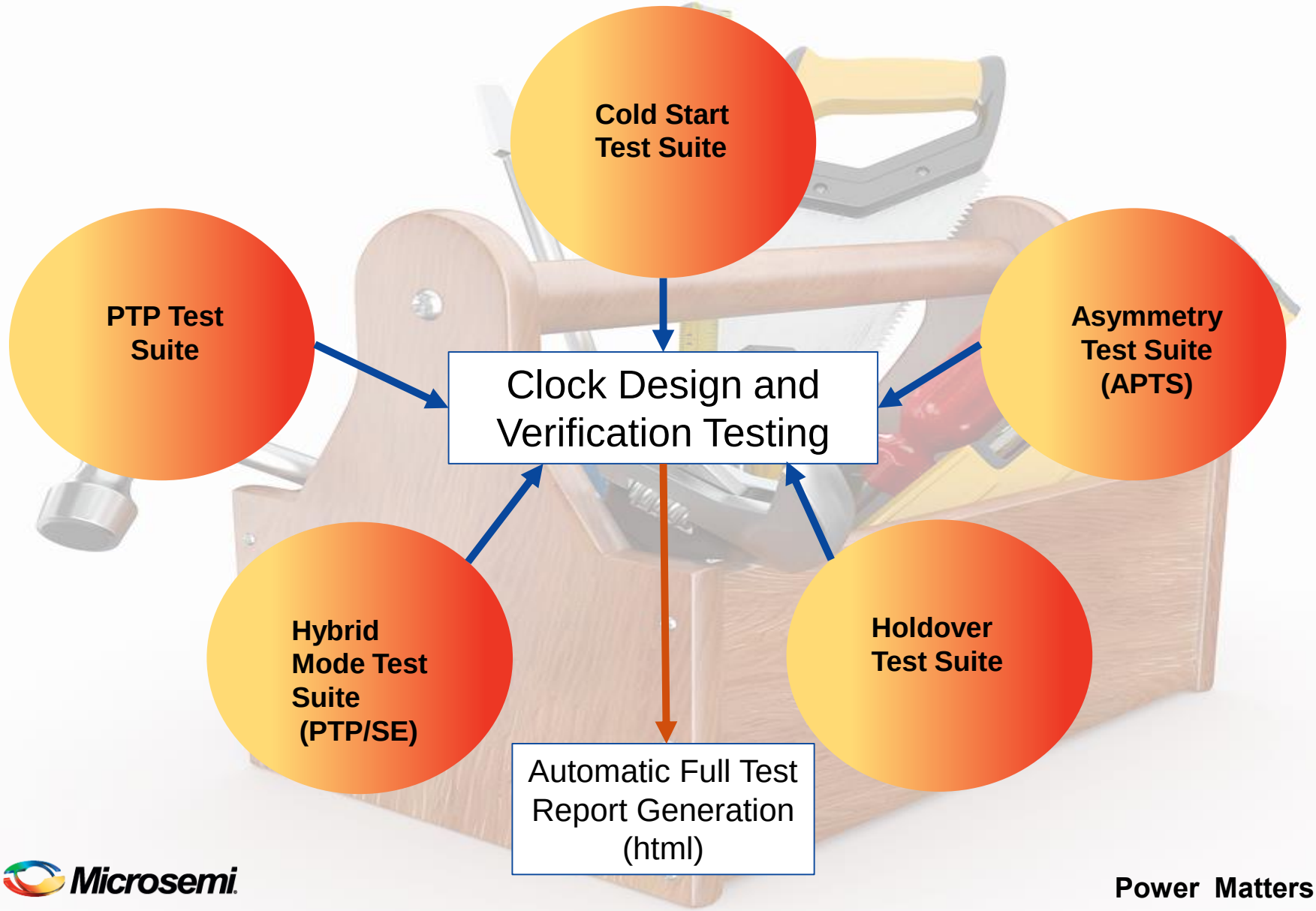
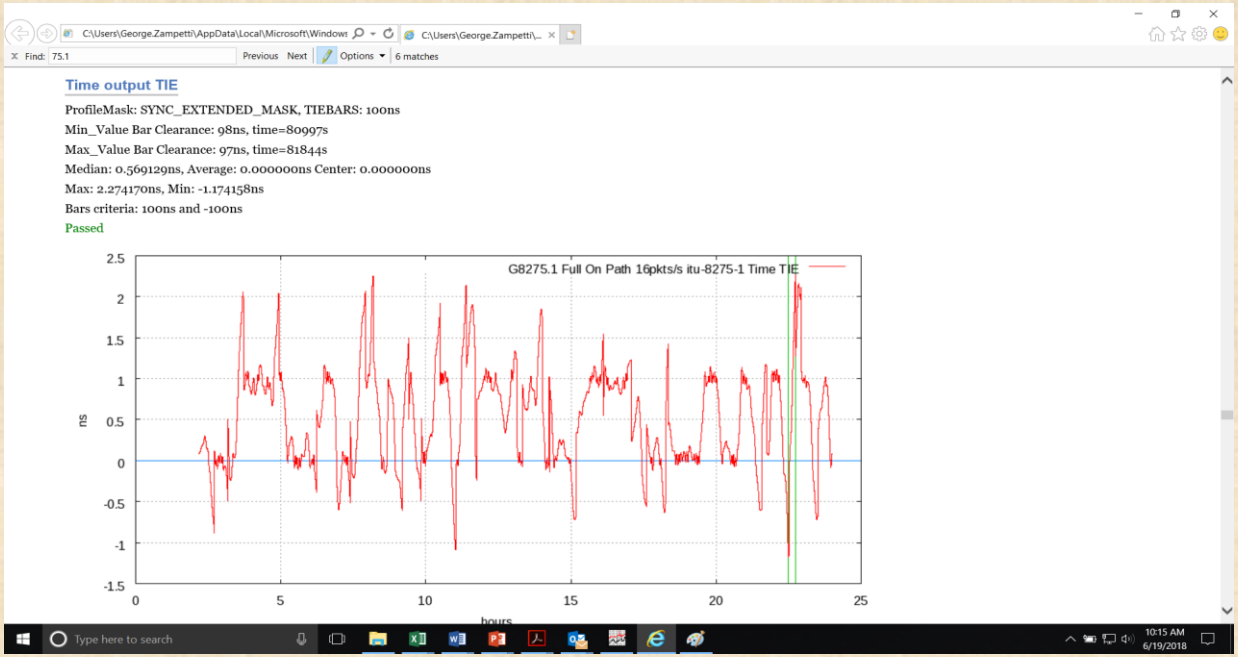
Overview of Clock Design and Verification Tool Kit



Overview of Clock Design Verification Test Suite

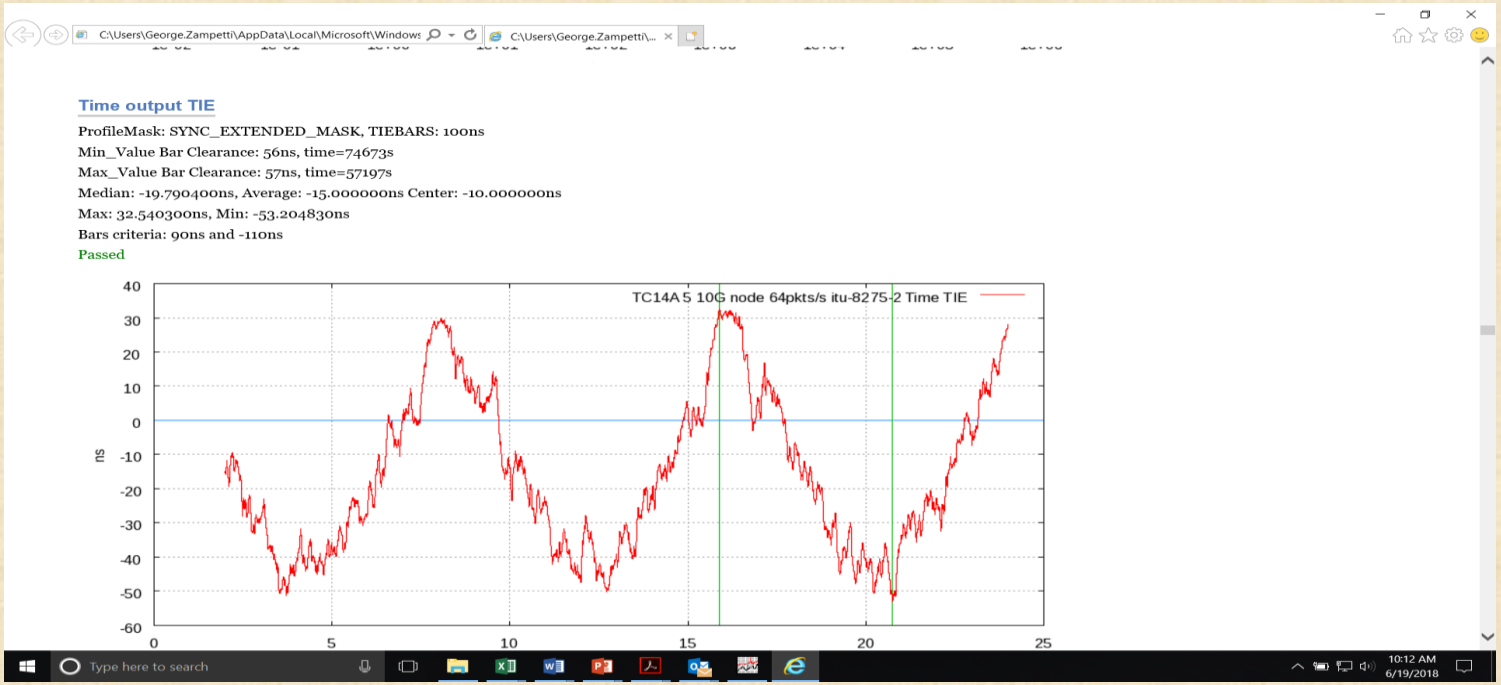


Clock Design Verification Test Suite in Operation



- Each Iteration of our Clock Algorithm is automatically tested for the complete test suite.
- Over 300 individual tests are currently performed covering over 6 months of total system test time.
- The 6 effective months of rigorous testing ensure consistent performance over all user deployment scenarios.
- The Verification Test Tools accomplished this testing in under 2 hours of real time.
- This slides show on example of the 300 tests (G8275.1 Wander Generation Case with Thermals)

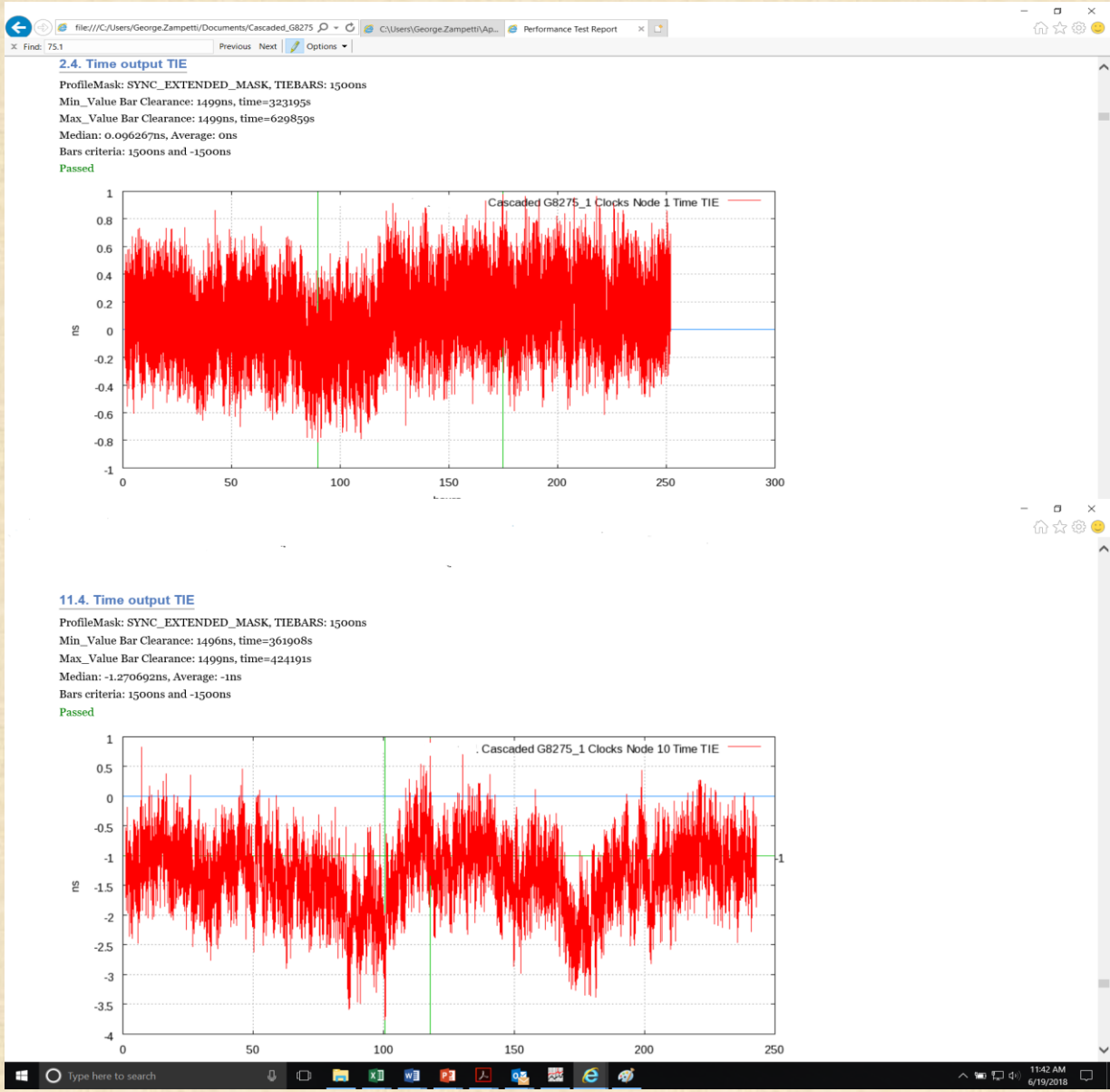
Clock Design Verification Performance of PTP over 10G bps example.



- This example shows performance of the latest clock algorithm over a realistic 75.2 PTP flow over 5 10Gbps Nodes.
- The test case is show with significant dynamic traffic load using the ITU standard benchmark test case 14 (G.8261).
- Interestingly while PTP over slower link experienced problems with time now a days high speed links support sub 100ns performance even without on path support

Clock Design Verification Test Suite Cascaded Clocks

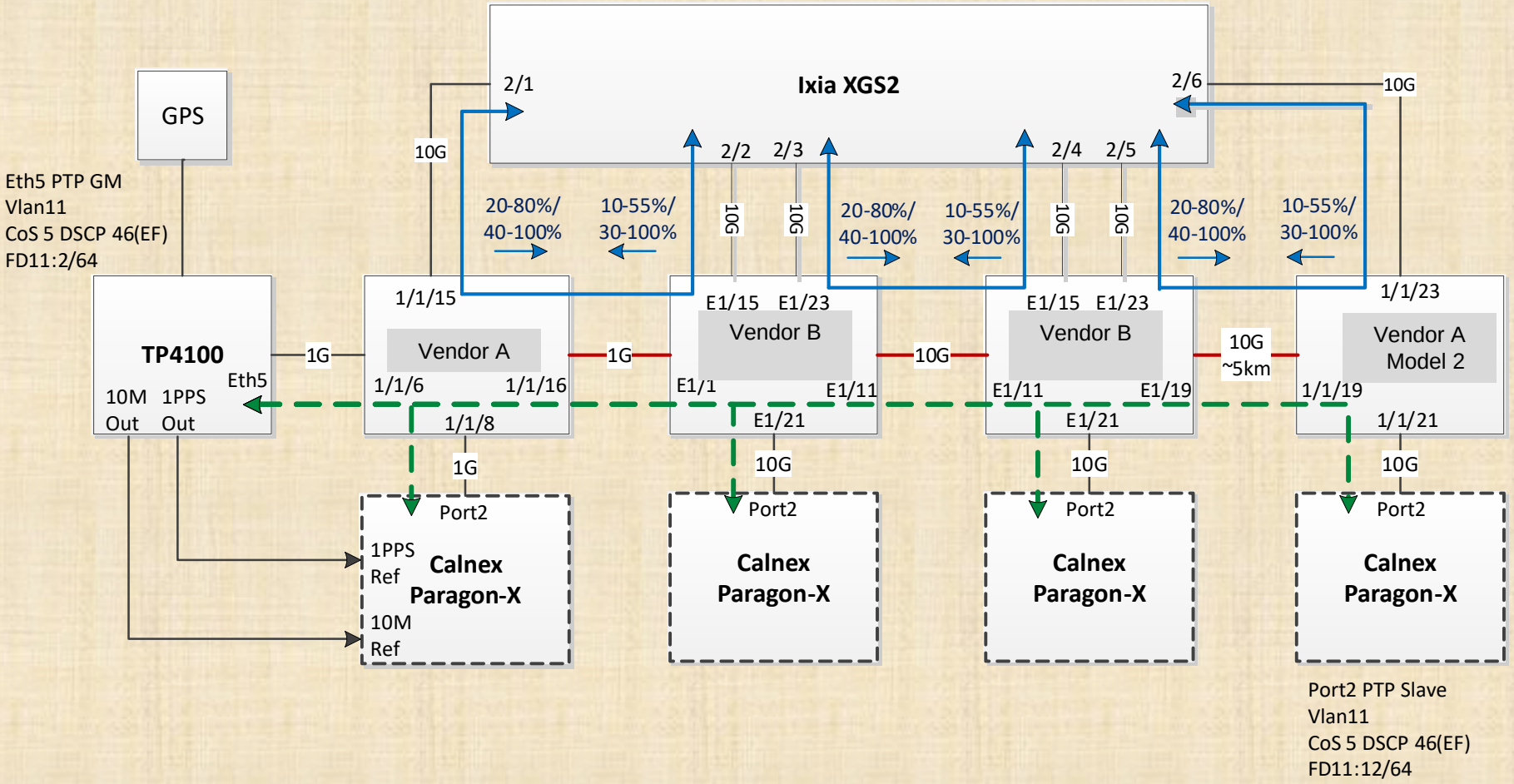
- Real World Deployments needs to look beyond a single clock to a cascaded chain of clocks and transport.
- The Clock Design tools support cascaded testing.
- This example show a chain of Microsemi Gateway Clocks operating in a full on path G8275.1 configuration.
- The top graph shows the time error a the first node and the bottom graph shows the tenth node
- Clearly with a properly designed gateway clock with a decent local oscillator the time error accumulation is insignificant.



Example User Case

- Investigate a particular set of current generation low latency routers and switches designed to support 5G backhaul.
- Focus is on no on-path support (G8275.2) as the performance of time transfer over these devices is expected to better than older lower speed routers and switches.

Testing Configuration



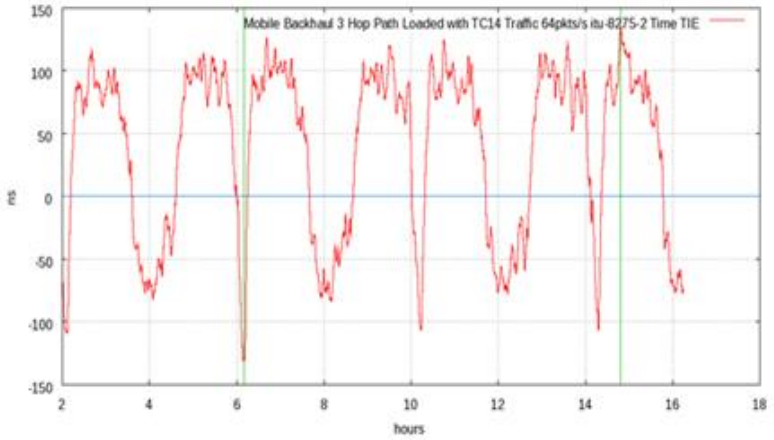
Constant Time Error Stats Summary – Port-to-Port Bias

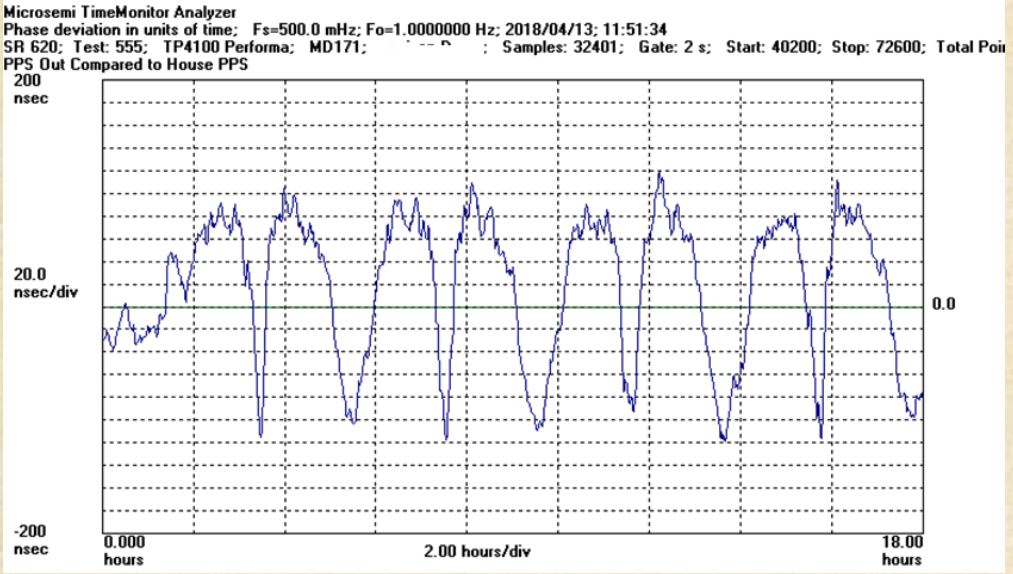
- Multiple port to port path configurations examined to understand asymmetry (constant errors) in these low latency switches and routers
- 6.1ns per node constant time error in comparison to ±50ns or ± 20ns per node by G.8273.2 (class A,B)
- Time error in nanosecond (ns)

	Entire Path	Per Node
Overall Mean	-18.29	-6.10
Standard Deviation	7.66	

Dynamic Time Error Stats Summary

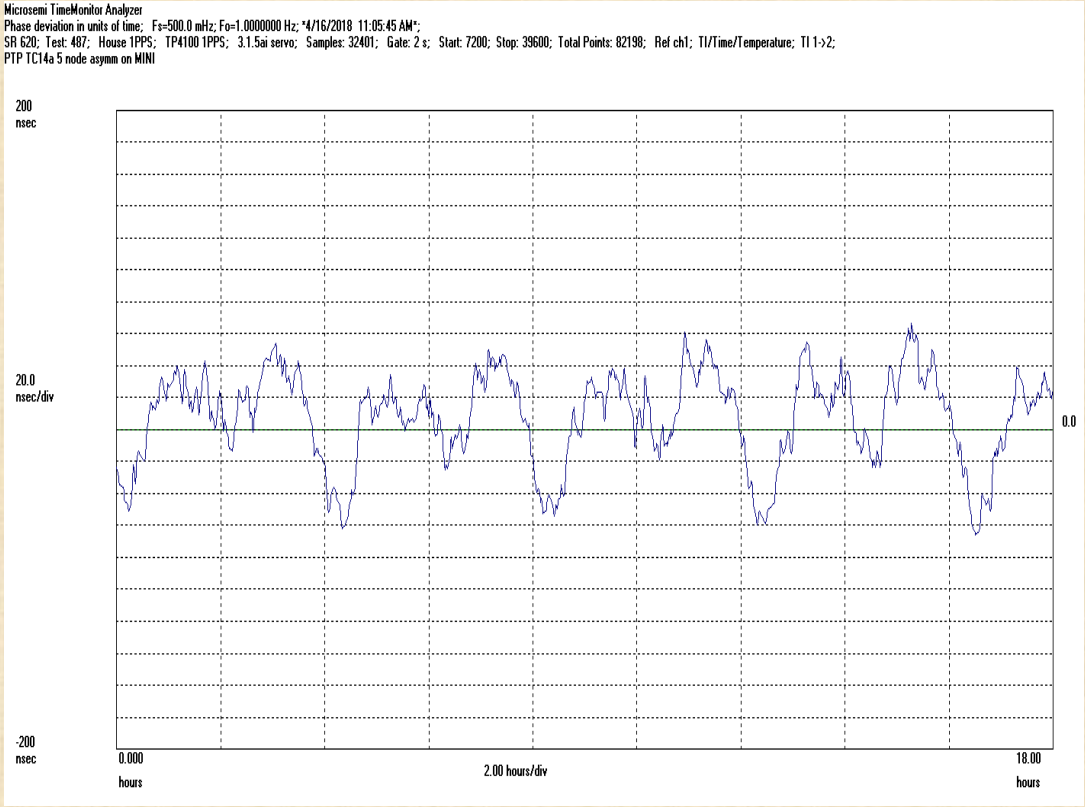
- The Packet Delay Variation playback files were captured and stored in the library.
- The playback feature was used in the design tools to generate the top graph time error results after several minutes
- The playback feature of the PDV test set was used to generate a faithful copy of the tested path into the TP4100 gateway clock and after 16 hours the bottom graph was obtained.
- Both results are in very good agreement and show that the dynamic error for this test case is 200ns.





Dynamic Time Error Stats Summary

- The same testing was performed with one adjustment (operating the 1Gbps first device with typical loading).
- The objective is to see the impact of the single slower speed device.
- As can be seen the dynamic error even under TC14 traffic stress is 100ns.



Summary

• Achieving consistent performance for time service over real world networks requires comprehensive support of many standards compliant configurations

• Tools to efficiently and comprehensively access the performance and critical to successful world deployment,

•Recent studies of current “5G” low latency switches and routers using these tools show significant time service improvement with no special on path support.